

# MS-7788 Ver: 1.0 u-ATX : 226 \* 173 mm

## CPU:

Intel - Sandy Bridge LGA 1155

## System Chipset:

INTEL - Cougar Point PCH(H61)

## OnBoard Chipset:

HD Audio Codec:ALC887VD / VT1708SCE

LAN:RTL 8105E 10/100 , Co-lay 8111E 10/100/1000

SIO:FIN71868AD

Flash ROM: 32Mb SPI (PCH)

## Main Memory:

DDRIII (1066/1333MHz) \* 2 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 1

## PWM:

Controller: UT501 3+1 Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: UP1504

CPU SA : OP+MOS

DDR: UP1504

PCH: OP+MOS

## ACPI:

UPI

## Other:

SATA2.0 x4 (PCH)

USB2.0 RearX6 Front x4

D-SUB/DVI\*1

TPM Header \*1

Speaker Pin Header

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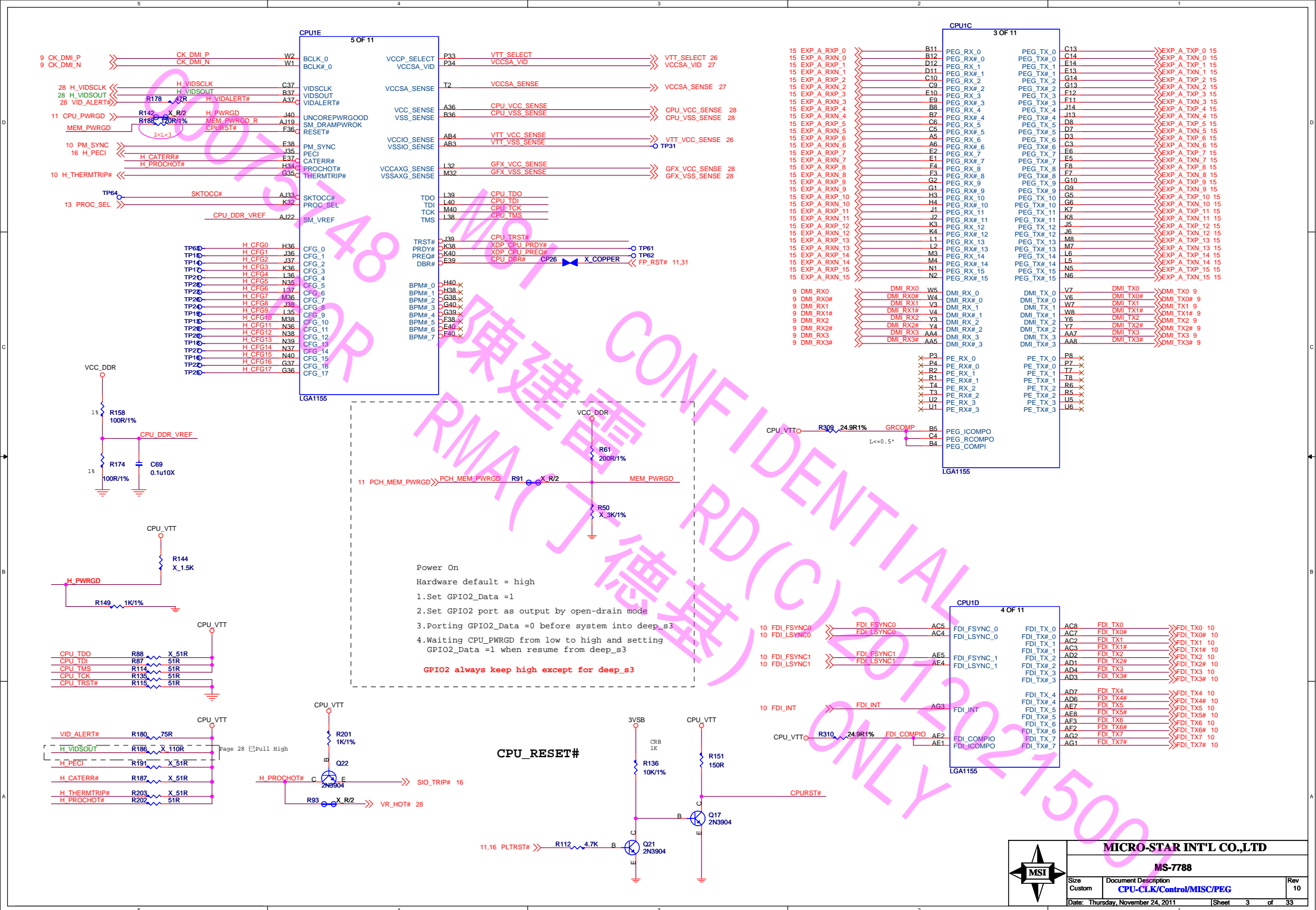


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MS-7788

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7 MEM\_MA\_ADD[15:0]

MEM\_MA\_ADD0 AV27  
MEM\_MA\_ADD1 AV24  
MEM\_MA\_ADD2 AW24  
MEM\_MA\_ADD3 AW23  
MEM\_MA\_ADD4 AV23  
MEM\_MA\_ADD5 AT24  
MEM\_MA\_ADD6 AT23  
MEM\_MA\_ADD7 AU22  
MEM\_MA\_ADD8 AV22  
MEM\_MA\_ADD9 AT22  
MEM\_MA\_ADD10 AV28  
MEM\_MA\_ADD11 AU21  
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MEM\_MA\_ADD13 AV32  
MEM\_MA\_ADD14 AU20  
MEM\_MA\_ADD15 AT20

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7 MEM\_MA\_WE\_L  
7 MEM\_MA\_CAS\_L  
7 MEM\_MA\_RAS\_L

MEM\_MA\_WE\_L AW29  
MEM\_MA\_CAS\_L AV30  
MEM\_MA\_RAS\_L AU28

SA\_WE#  
SA\_CAS#  
SA\_RAS#

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7 MEM\_MA\_BANK2

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MEM\_MA\_BANK1 AW28  
MEM\_MA\_BANK2 AV20

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SA\_BS\_2

7 MEM\_MA\_CS\_L0  
7 MEM\_MA\_CS\_L1

MEM\_MA\_CS\_L0 AU29  
MEM\_MA\_CS\_L1 AV32

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7 MEM\_MA\_CKE0  
7 MEM\_MA\_CKE1

MEM\_MA\_CKE0 AV19  
MEM\_MA\_CKE1 AT19

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7 MEM\_MA\_ODT0  
7 MEM\_MA\_ODT1

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7 MEM\_MA\_CLK\_H0  
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7 MEM\_MA\_CLK\_L1

MEM\_MA\_CLK\_H0 AY25  
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7,8 DOR3\_DRAMRST#

R295 X\_R2 DOR3\_RST# AW18

SM\_DRAMRST#

C235 X\_0.1u16X

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LGA1155

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AE3 MEM\_MA\_DATA63

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MEM\_MA\_DQS\_H63

CPU1B 2 OF 11

8 MEM\_MB\_ADD[15:0]

MEM\_MB\_ADD0 AK24  
MEM\_MB\_ADD1 AM20  
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MEM\_MB\_ADD3 AK18  
MEM\_MB\_ADD4 AP19  
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MEM\_MB\_ADD8 AN18  
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MEM\_MB\_ADD15 AV16

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SB\_MA\_15

8 MEM\_MB\_WE\_L  
8 MEM\_MB\_CAS\_L  
8 MEM\_MB\_RAS\_L

MEM\_MB\_WE\_L AR25  
MEM\_MB\_CAS\_L AK25  
MEM\_MB\_RAS\_L AP24

SB\_WE#  
SB\_CAS#  
SB\_RAS#

8 MEM\_MB\_BANK0  
8 MEM\_MB\_BANK1  
8 MEM\_MB\_BANK2

MEM\_MB\_BANK0 AP23  
MEM\_MB\_BANK1 AM24  
MEM\_MB\_BANK2 AW17

SB\_BS\_0  
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SB\_BS\_2

8 MEM\_MB\_CS\_L0  
8 MEM\_MB\_CS\_L1

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MEM\_MB\_CS\_L1 AN26

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8 MEM\_MB\_ODT0  
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7,8 DOR3\_DRAMRST#

R295 X\_R2 DOR3\_RST# AW18

SM\_DRAMRST#

C235 X\_0.1u16X

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LGA1155

MEM\_MB\_DATA[63:0] 8

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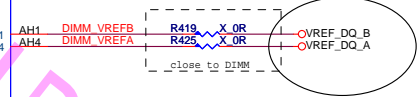
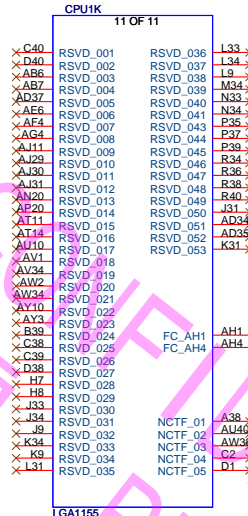
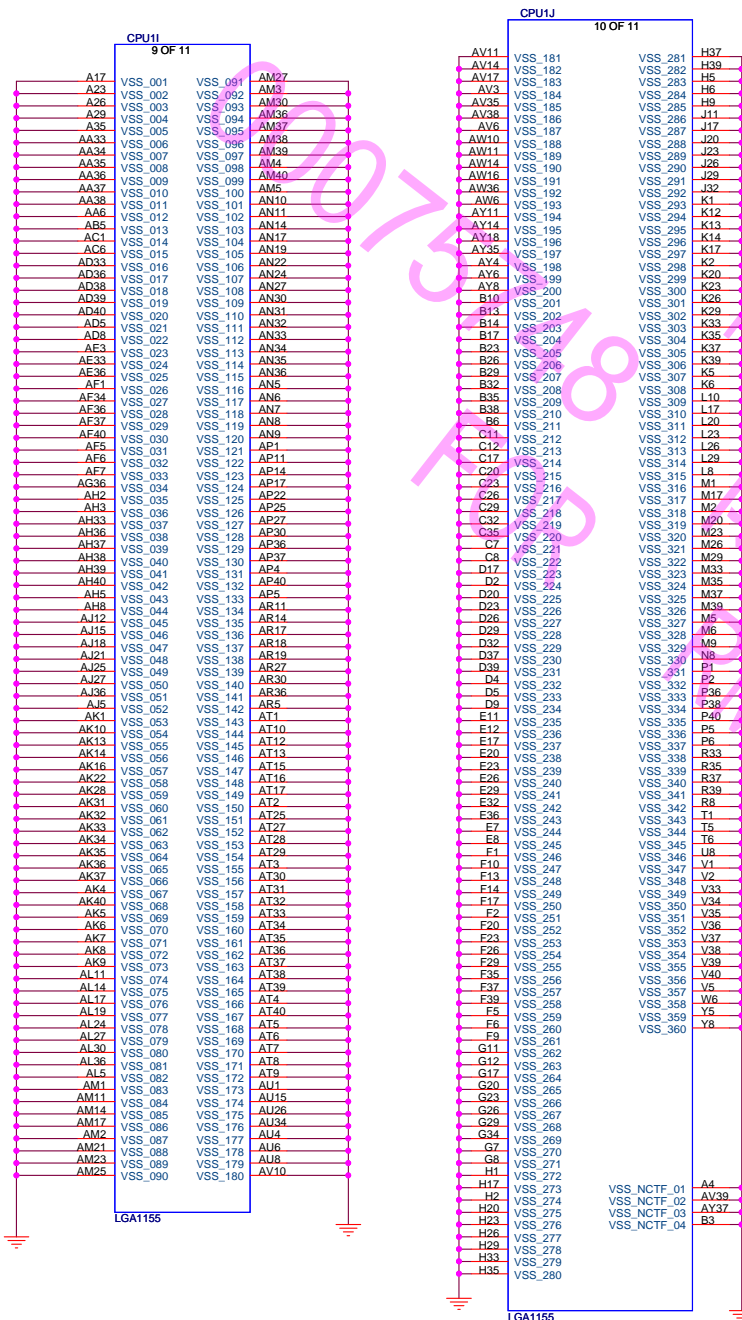
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Size	Document Description	Rev
Custom	CPU-Memory	10

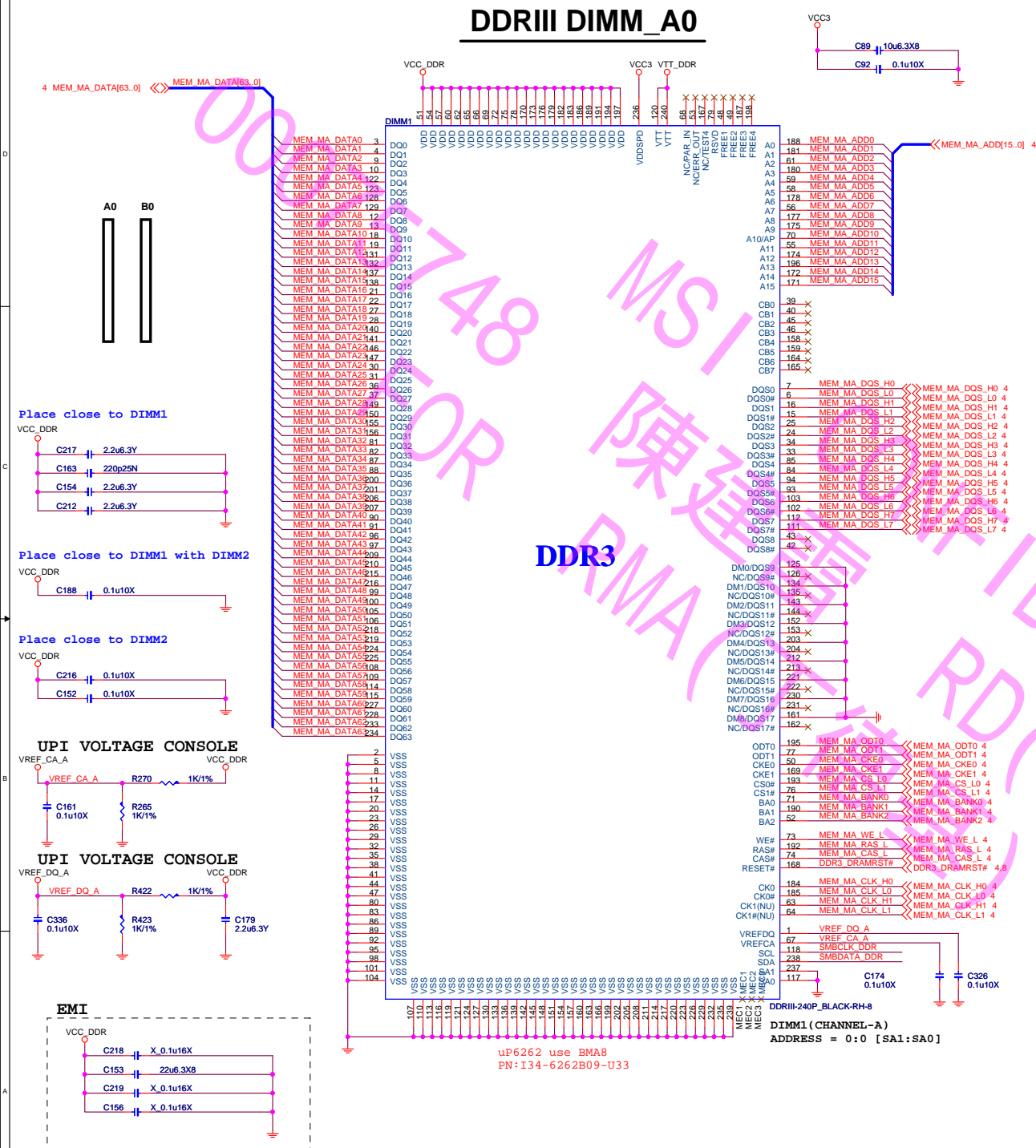
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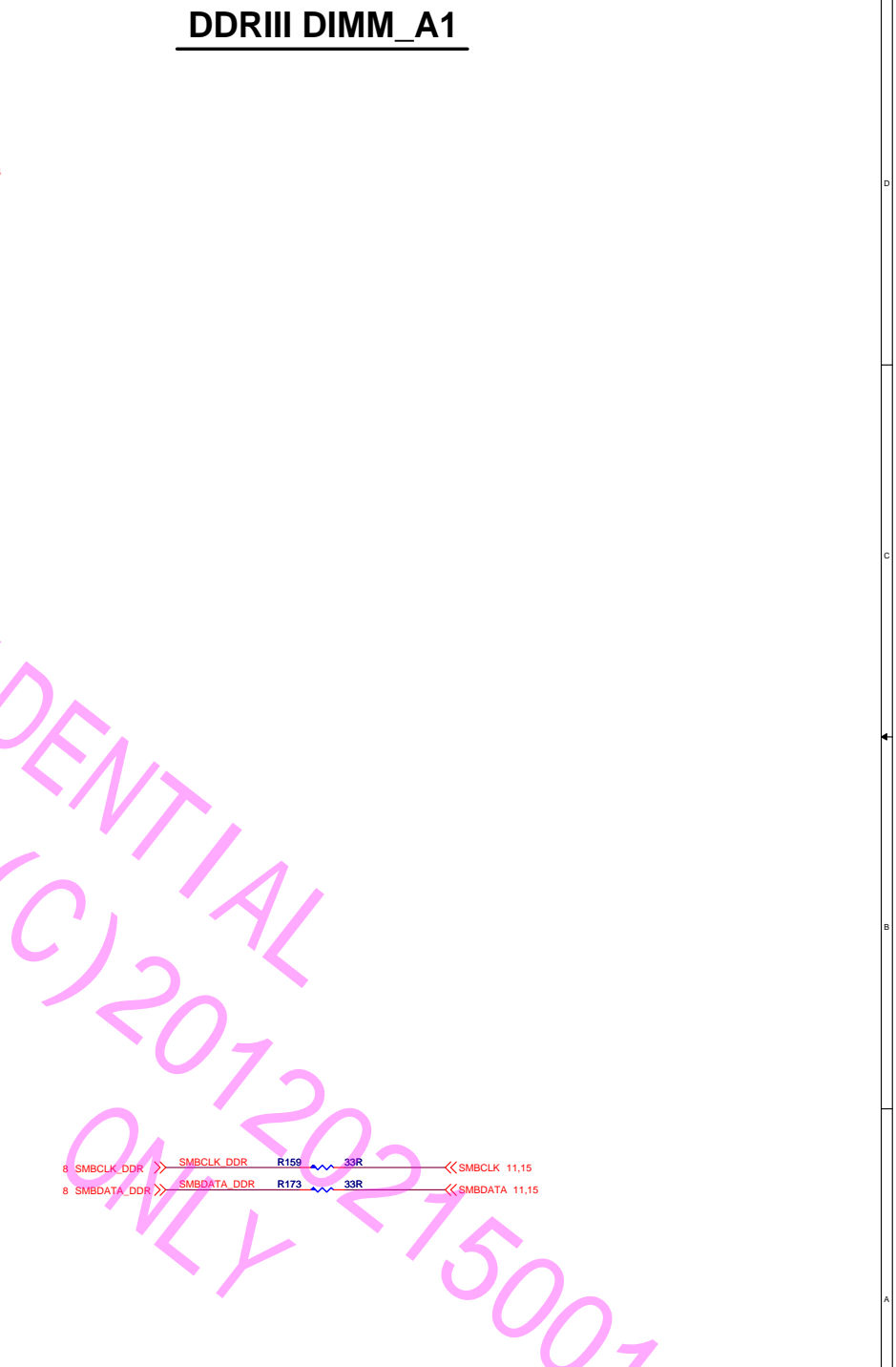




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## DDRIII DIMM\_A1

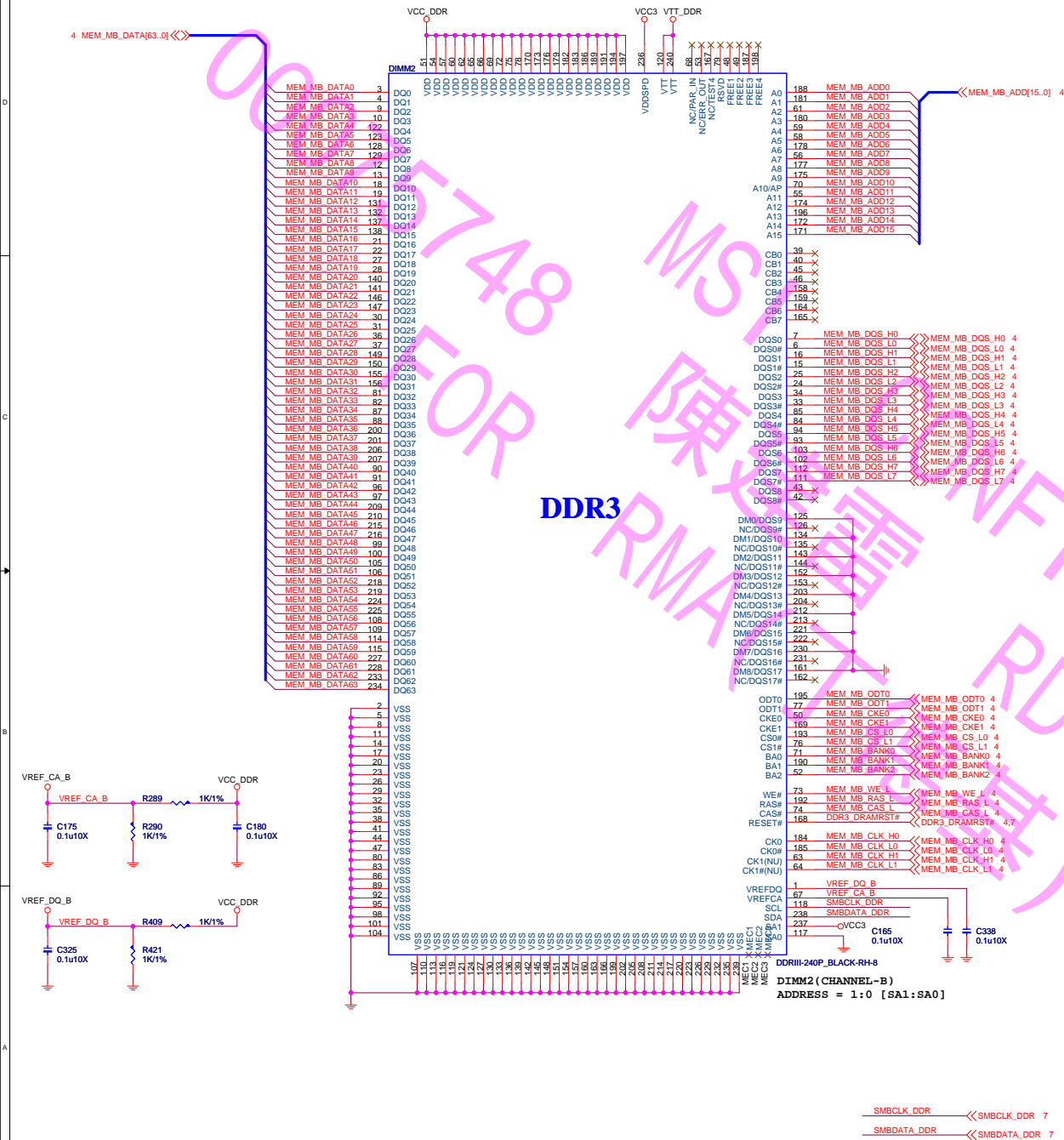


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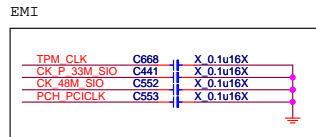
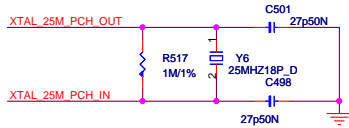
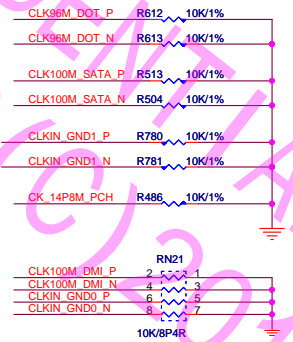
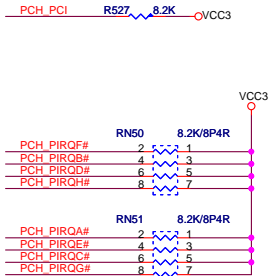
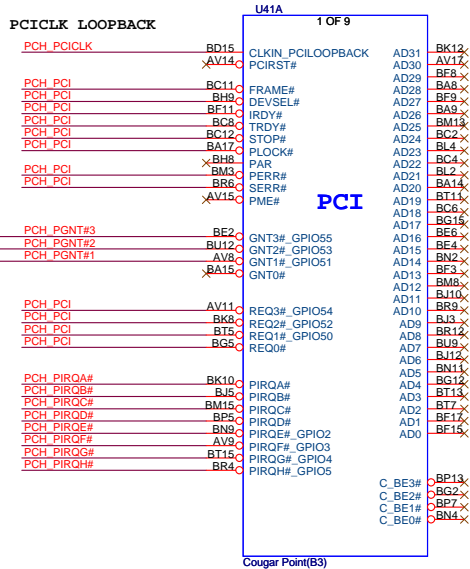
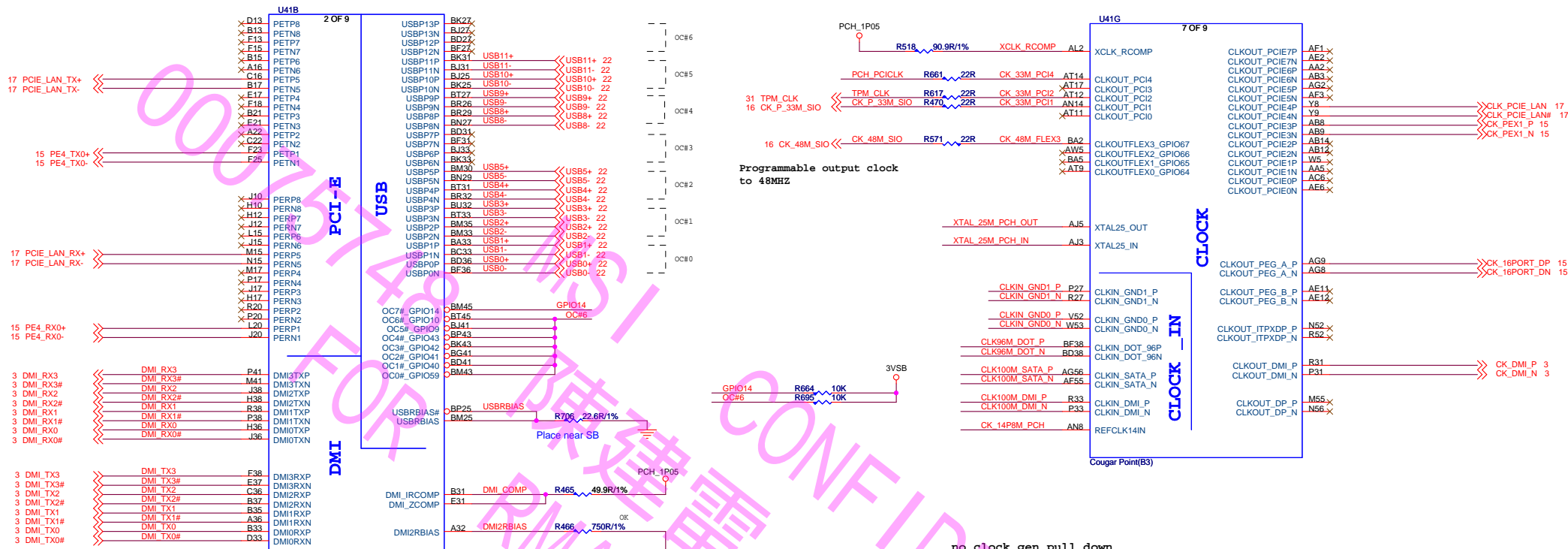
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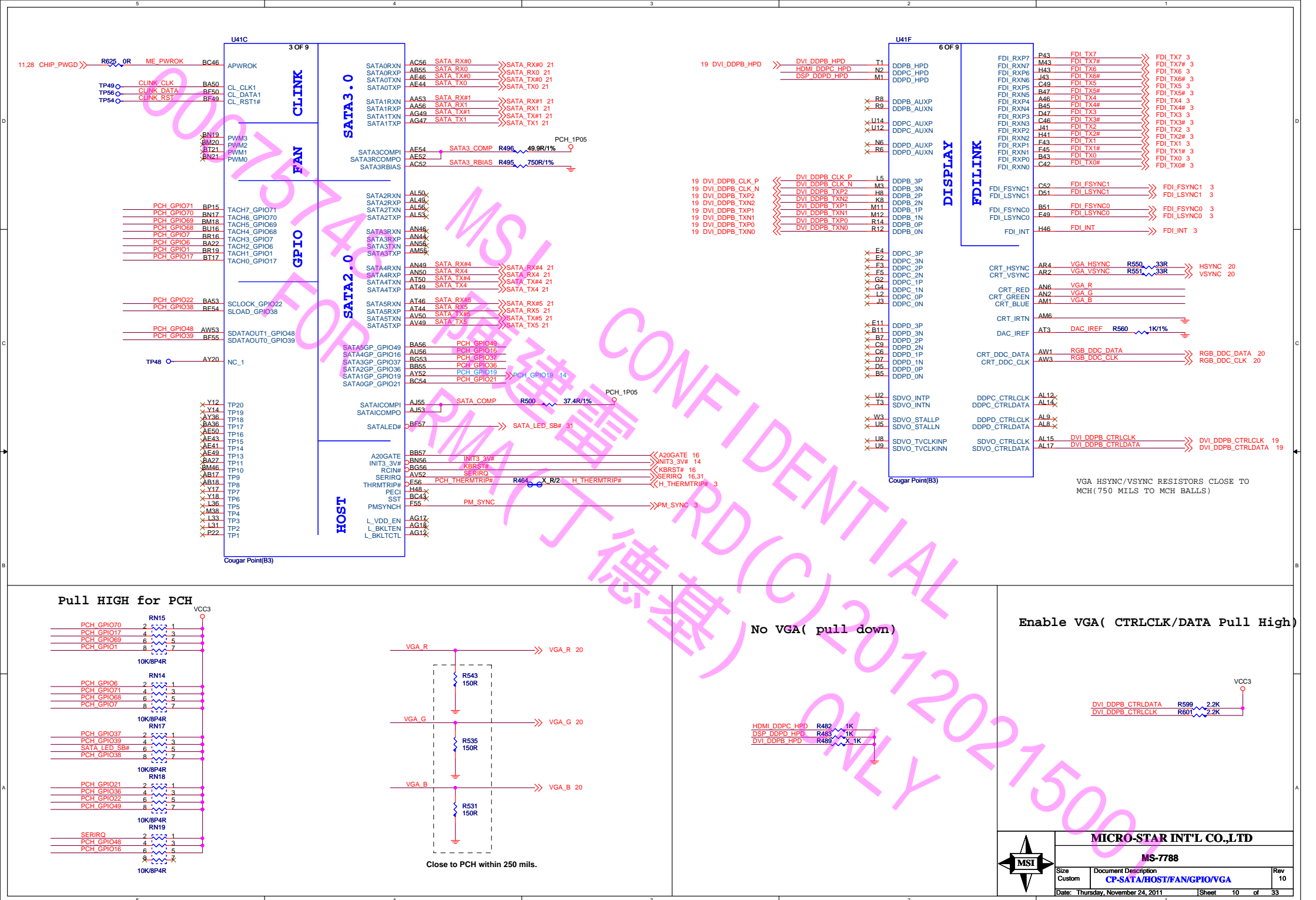
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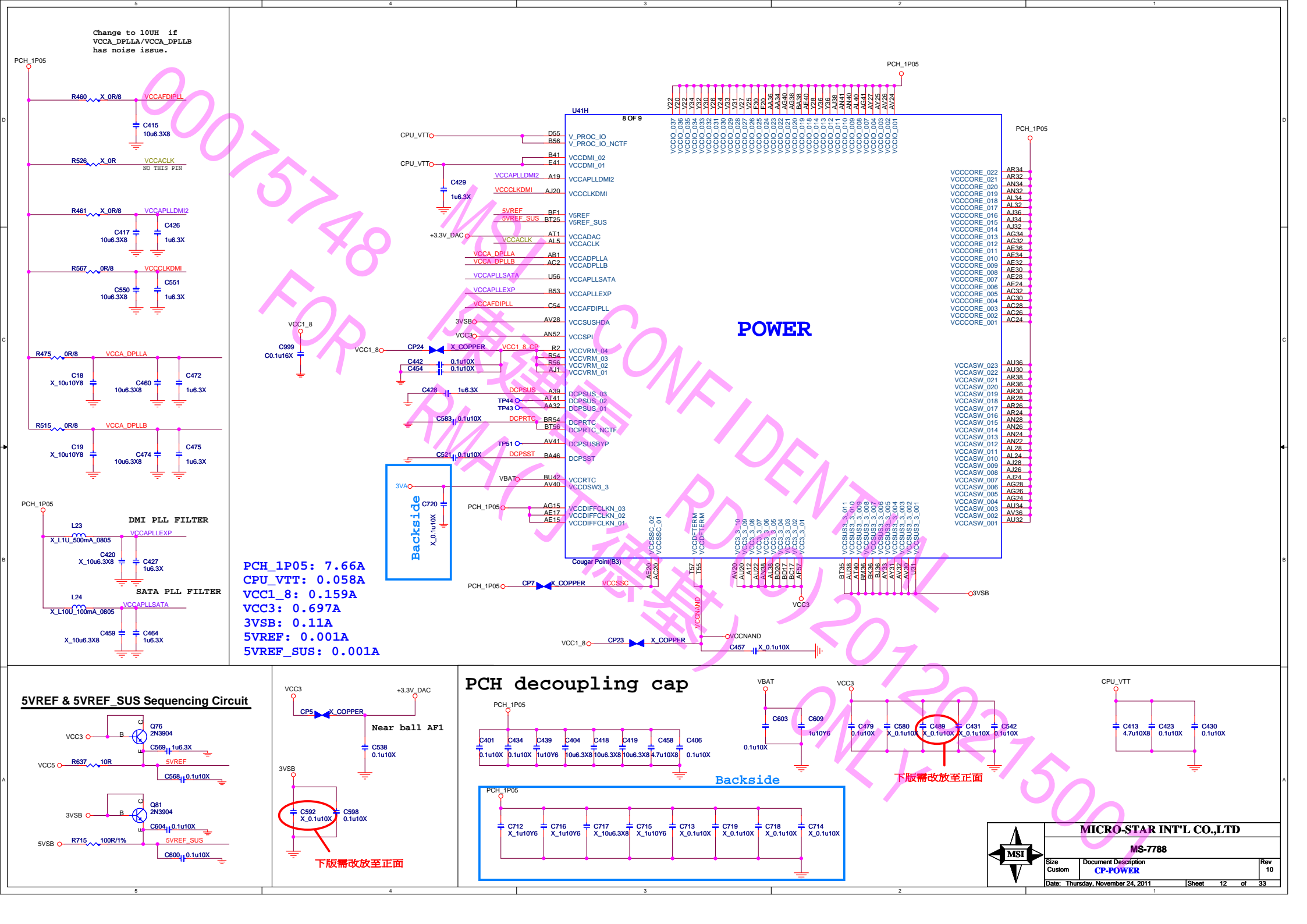
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SMBDATA\_DDR << SMBDATA\_DDR 7

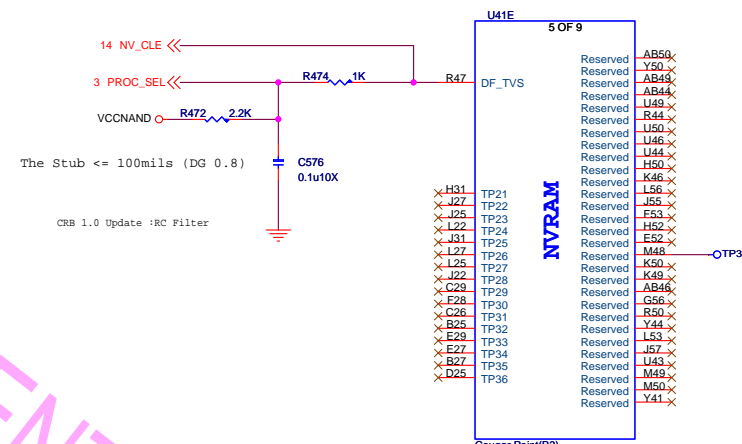
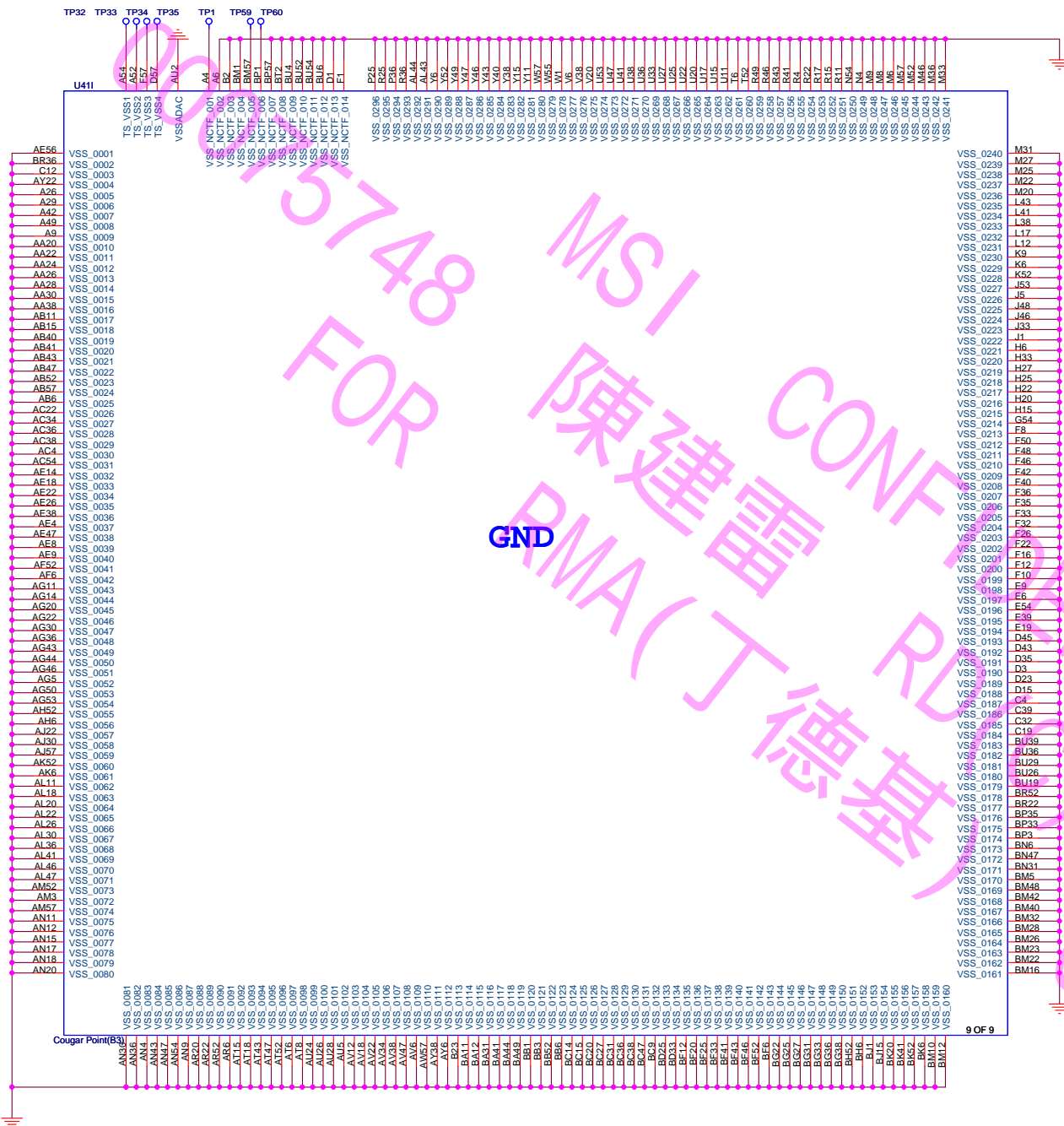








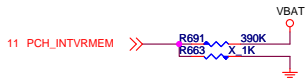
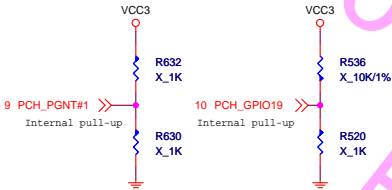






PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



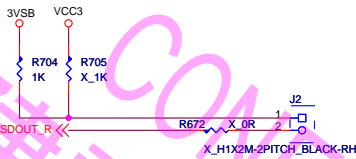
INTVRMEN  
0: DISABLE INTERNAL VRM  
1: ENABLE INTERNAL VRM \*

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



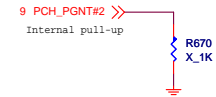
DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

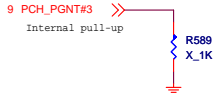


HDA\_SDO  
Disable ME in Manufacturing Mode when pull LOW ????

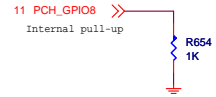
HDA\_SDO has internal pull down.  
Default should be connected to SDIN of codec, no pull up/down.  
To Disable ME need to have a jumper to pull high



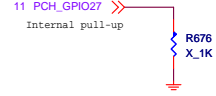
DMI AC/DC MODE  
0 : AC  
1 : DC \*



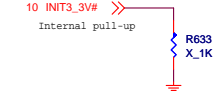
Topblock swap override when pull-low  
Signal has a weak internal pull-up



GPIO8  
0 : Integrated Clocking Enable (FCIM)\*  
1 : Buffer Through Mode Enable (BTM)

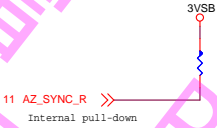


GPIO28  
0 : OD PLL VR disabled  
1 : OD PLL VR enabled \*  
Signal has a weak internal pull-up



INIT3\_3V#  
0 : ??????????????  
1 : ?????????????? \*

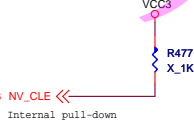
1: INIT3\_3V to asserted for 16 PCI clock to reset the processor by some evens occur.  
0: Can not to reset the processor.



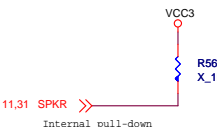
HDA\_SYNC  
OD PLL VR SUPPLY SEL  
0: 1.8V SUPPLY \*  
1: 1.5V SUPPLY



GPIO15  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*?  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



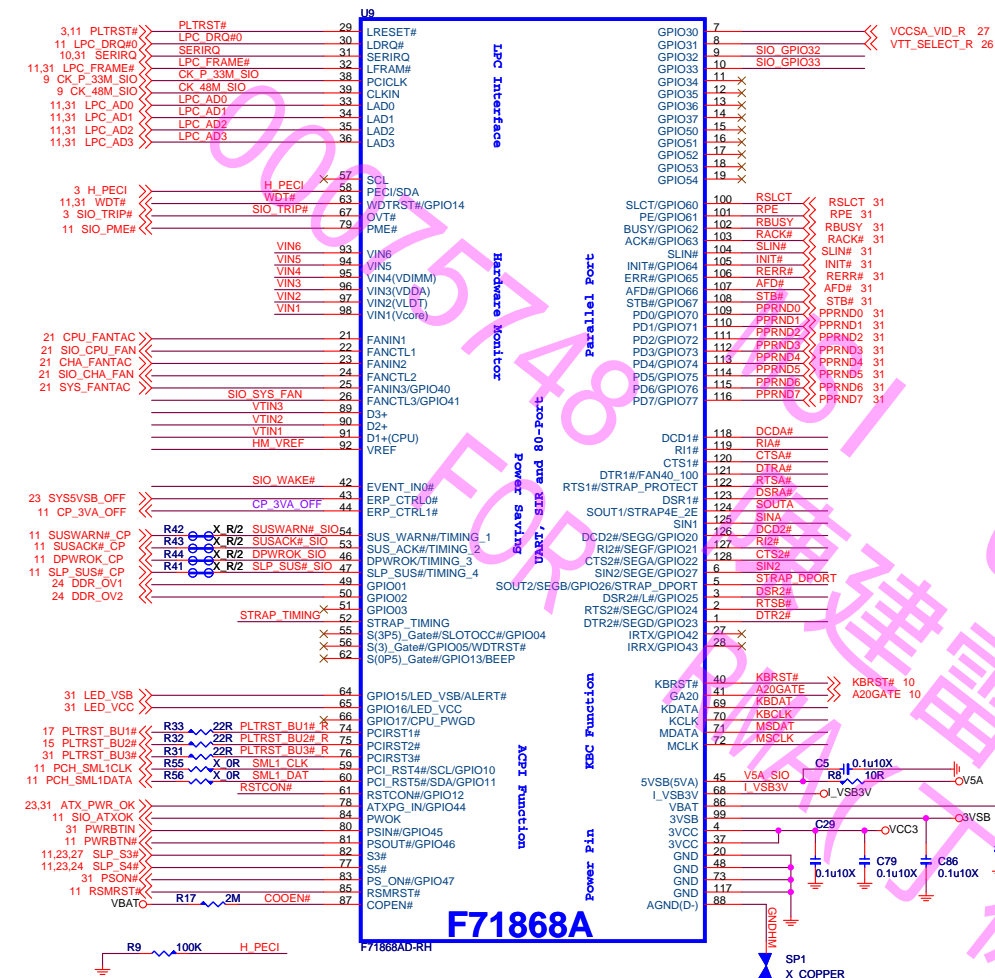
SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT



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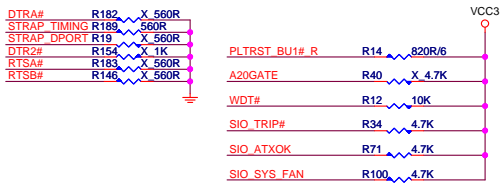


# LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

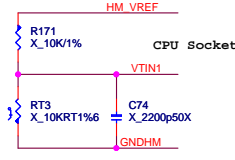
STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courager point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
Strap_Peotect (RTSA#)	Alarm mode	Force mode

MB ID	GPIO 32	33
SKU_A	0	0
	0	1
	1	0
	1	1

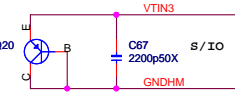
# OPT BOM



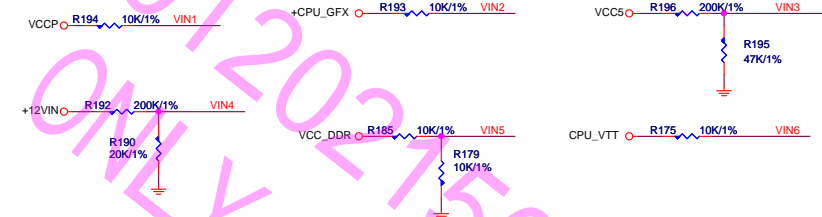
# HW Monitor - Thermal



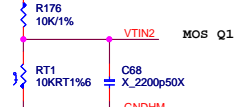
# Close to Hot point



# HW Monitor - Voltage



# HW Monitor - Voltage

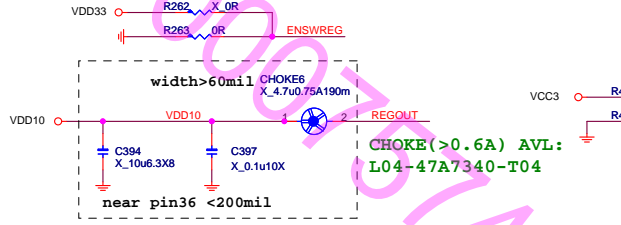


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# Power Regulator Option

	Mode	Choke6	C394	C397	C414	C421	R262	R263
8111E Series & 8105E Series	SWR mode							
8105E Series	LDO mode							

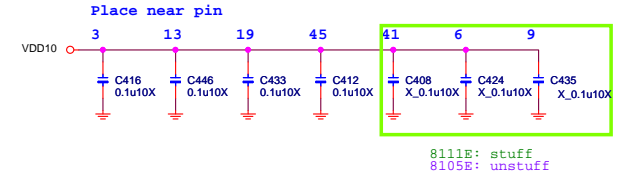
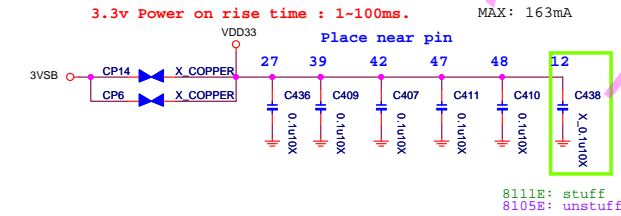
# RTL8105E 10/100M LAN co-lay RTL8111E Giga LAN



## For RTL8111E Series EEPROM / ASF / Efuse Function

	EEPROM 93C46	EEPROM 93C56/603C46	EEPROM 93C46	EFuse
SMBCLK	X	X	L	X
SMBDATA	L	H	H	L
GPO	H	H	H	H

Note: For RTL8111E-VL, R17 must be 1K.

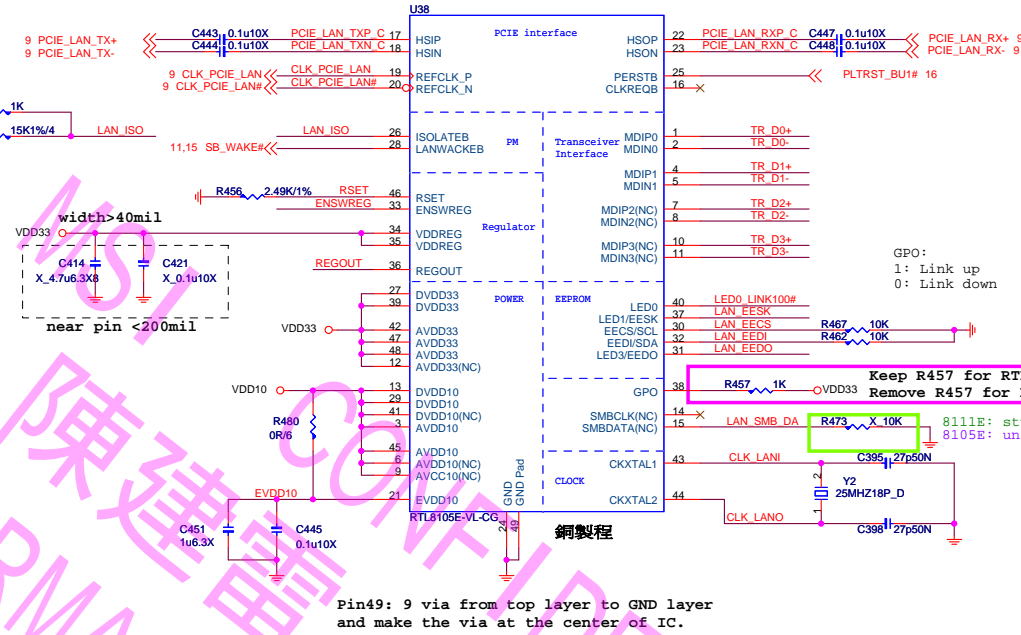


## 8105E POWER Consumption

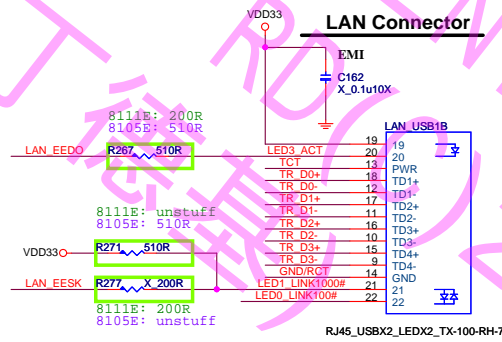
	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

## 8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



## LAN Connector



Giga-Lan	10/100-Lan
<b>N58-22F0731</b> Link Yellow Active Blinking 1000 Orange 100 Green 10 None	<b>N58-22F0771</b> Link Yellow Active Blinking 100 Green 10 None
19 20 21 22	19 20 21 22



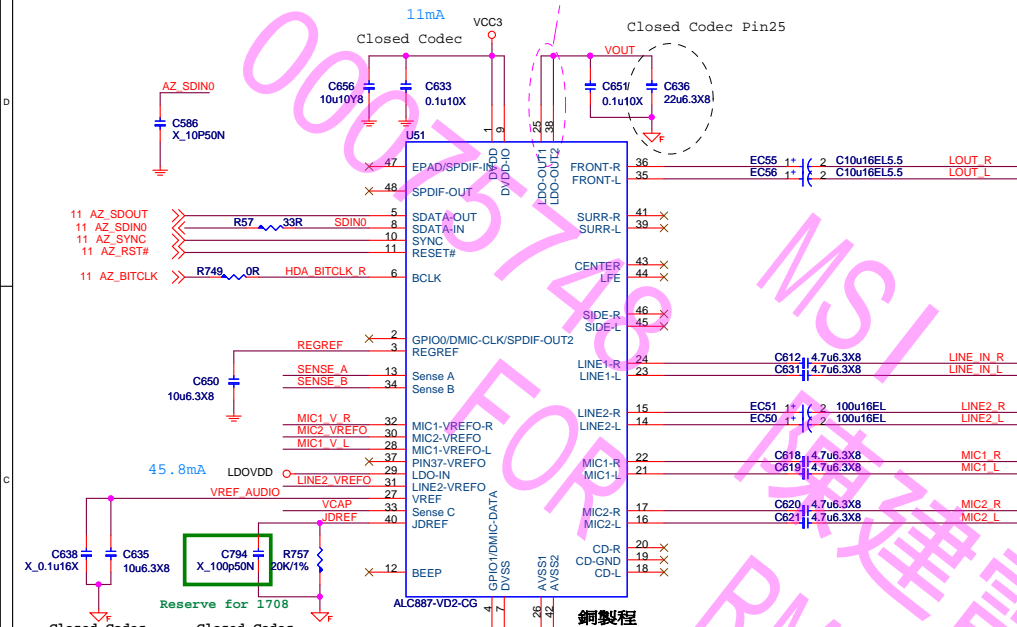
MICRO-STAR INT'L CO.,LTD

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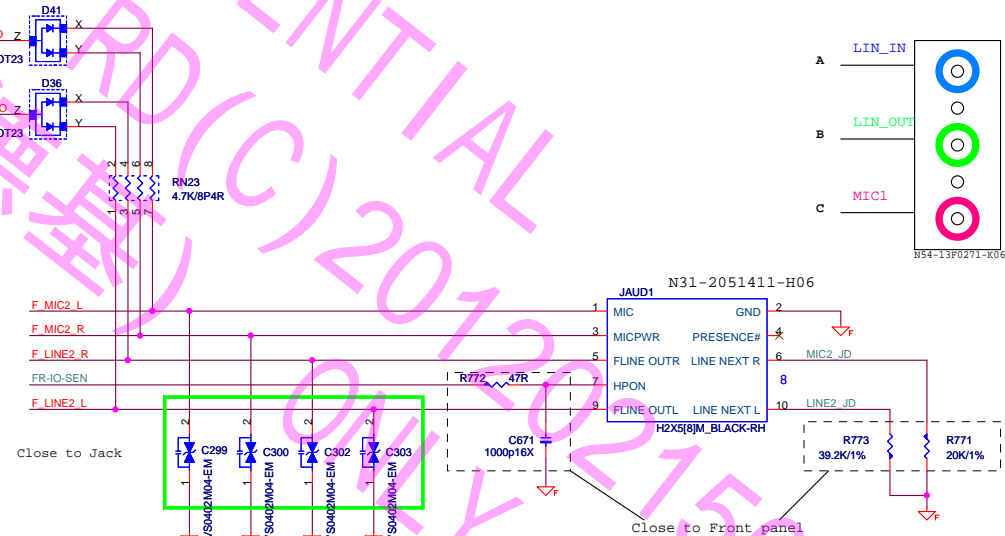
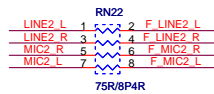
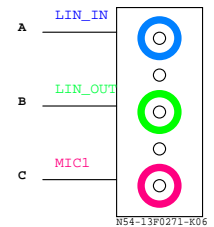
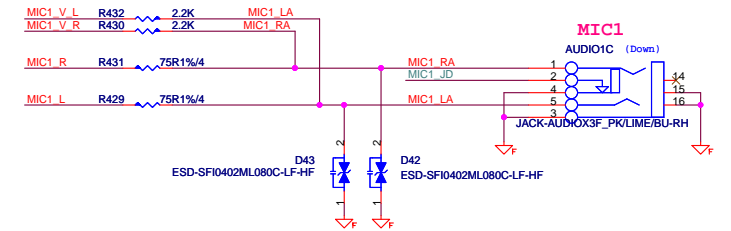
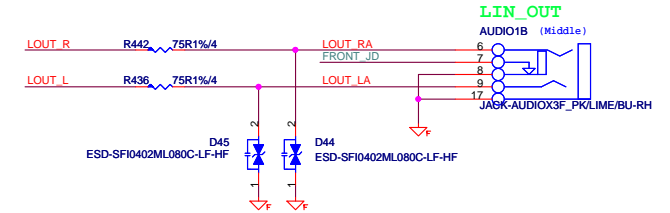
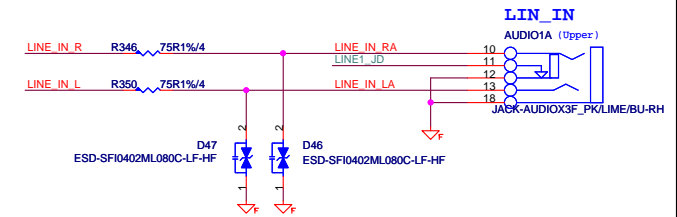
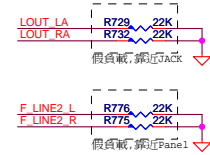
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ALC887-VD  
VT1708S CE

Codec Pin25 & 38連接的Layout，以最短路徑，至少40mils線寬連接。



當串接電容有極性時，需上對地電阻

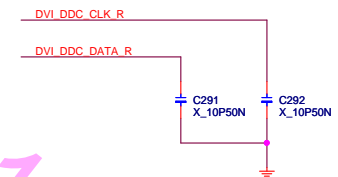
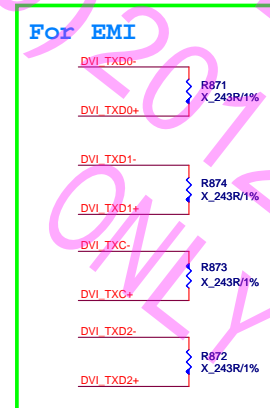
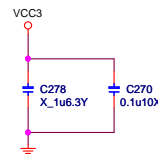
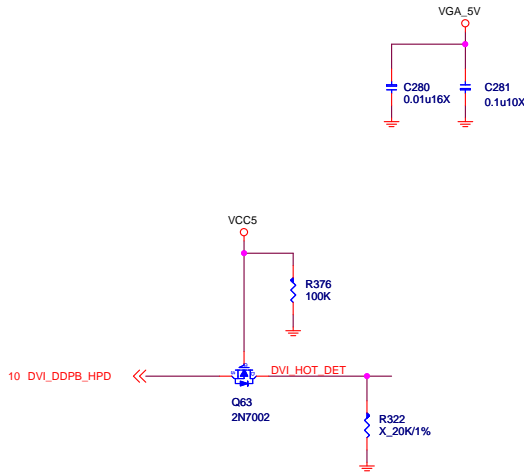
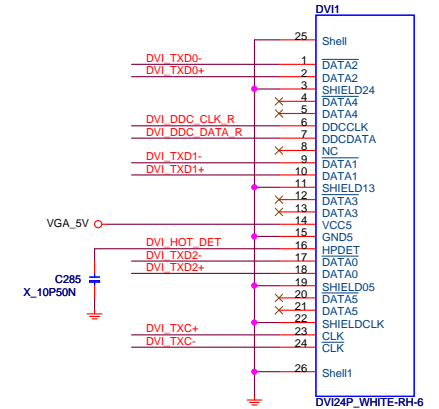
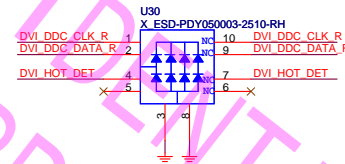
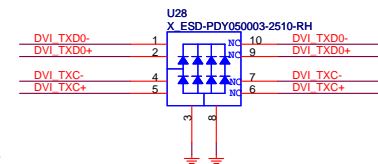
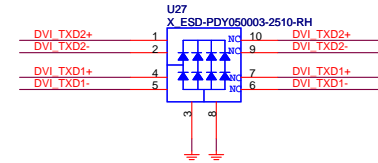
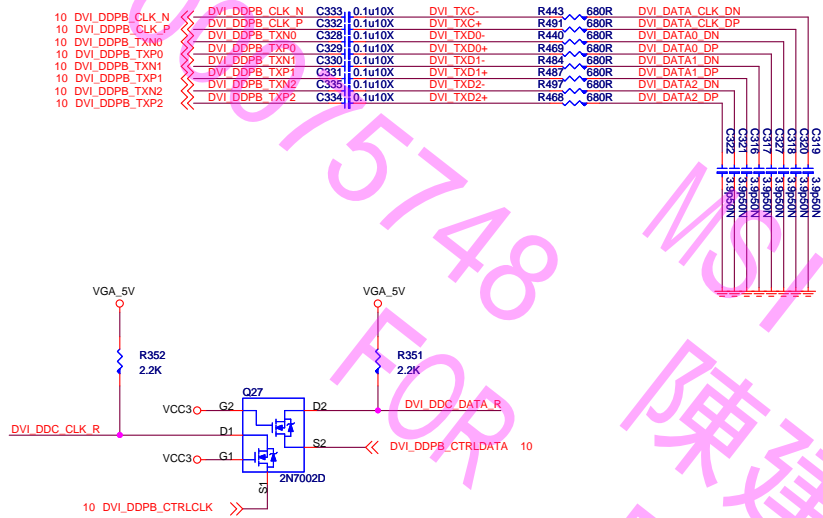


Varister --> cap for cost down

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# DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift

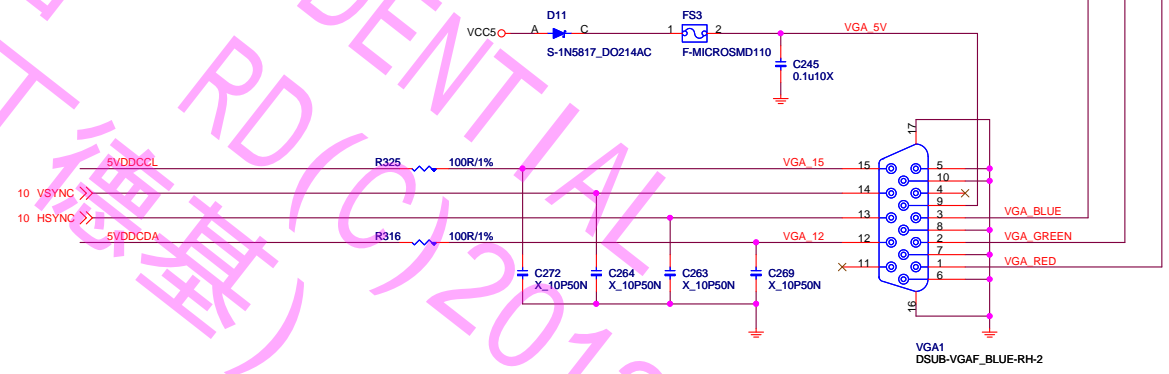
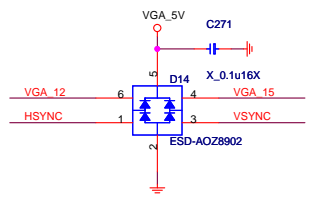
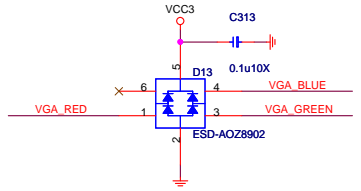
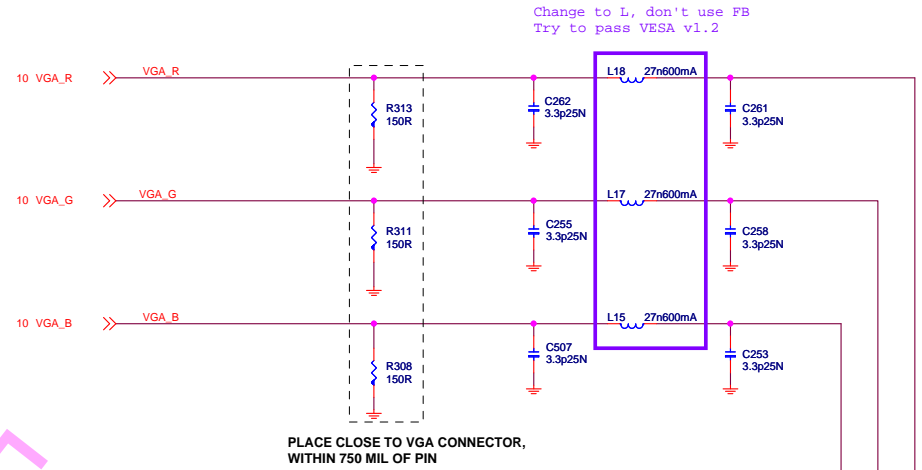
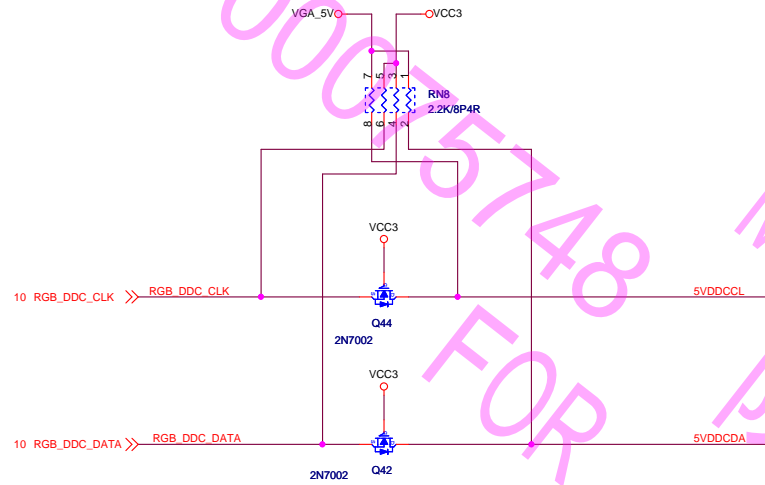




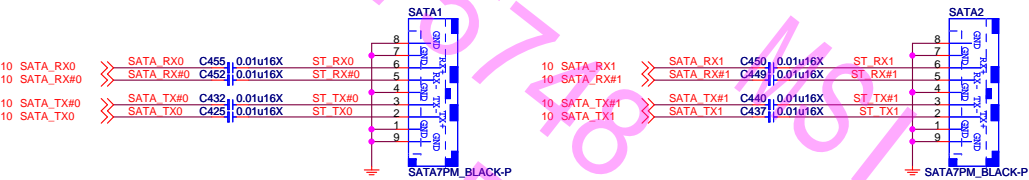
Table 1-3. Desktop Intel® 6 Series Chipset SKUs

Feature Set	SKU Name(s)					
	Q67	Q65	B65	H67	P67	H61
Total number of SATA ports	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 <sup>4</sup>	1 <sup>5</sup>	1 <sup>5</sup>	2 <sup>4</sup>	2 <sup>4</sup>	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4 <sup>8</sup>

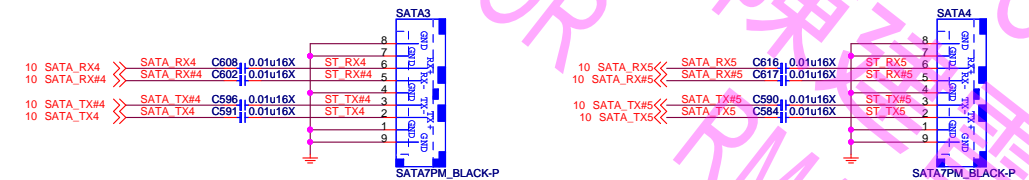
NOTES:

8. SATA ports 2 and 3 are disabled.

SATA 3G PORT 0,1

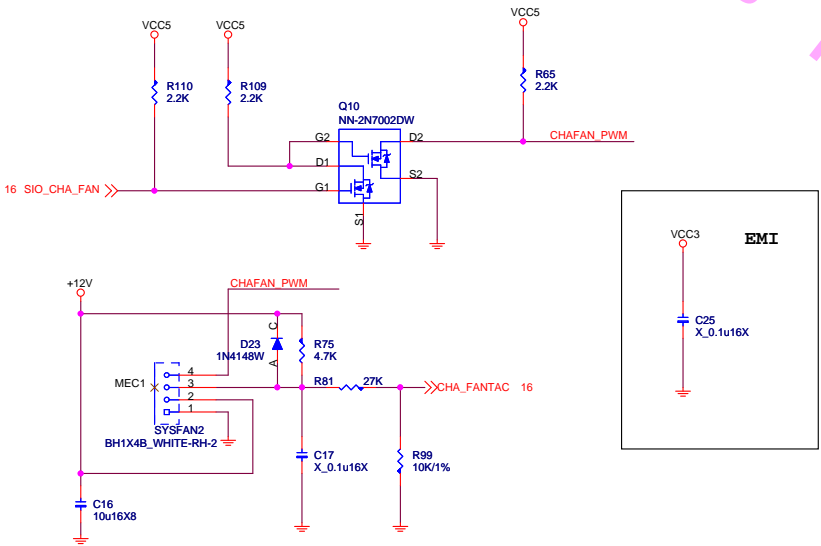


SATA 3G PORT 4,5



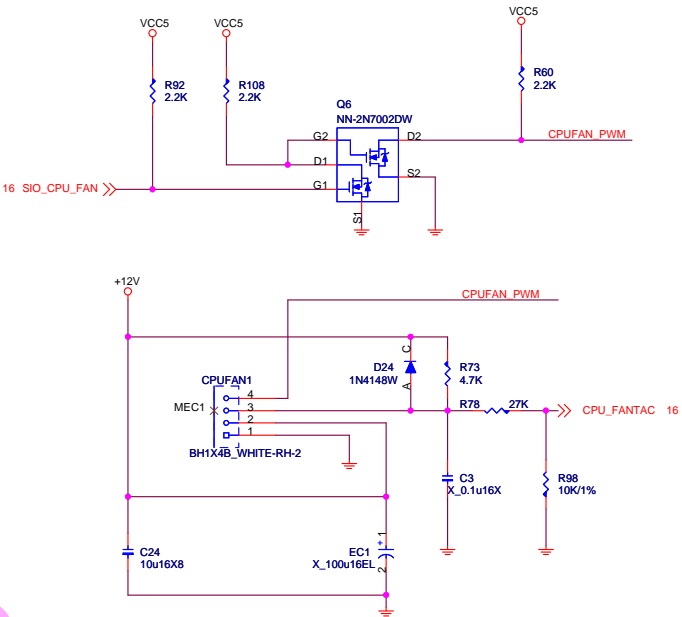
CHASSIS FAN-COUNTROL CIRCUIT

From SIO SYSTEM FAN2



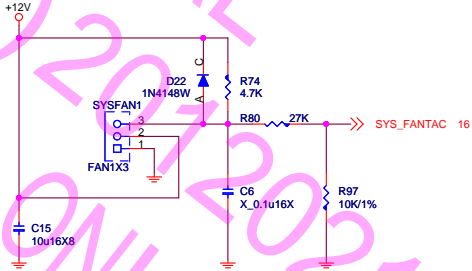
CPU FAN-COUNTROL CIRCUIT

From SIO SYSTEM FAN1



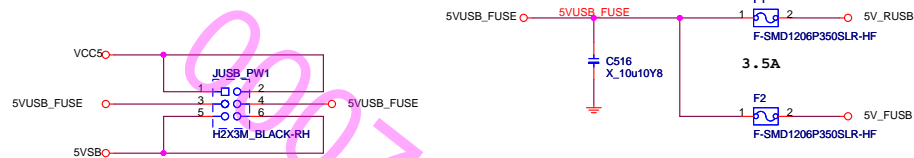
SYSTEM FAN3-COUNTROL CIRCUIT

From SIO SYSTEM FAN3



## 5V\_RUSB Switch

5V\_RUSB must 120mm



Default VCC5 (PIN1-3,2-4)

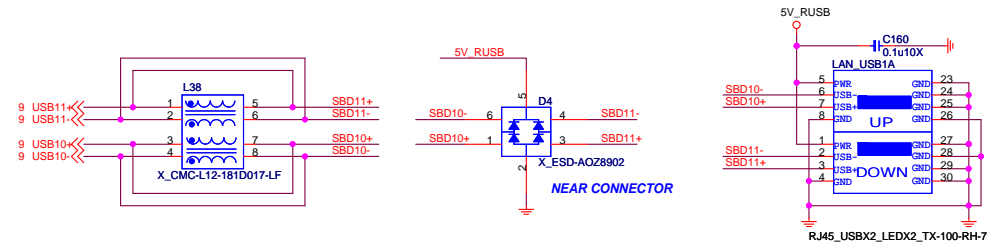
JUSB_PW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
	EUP Disable	Not support
3-5,4-6	EUP Enable	Not support
	EUP Disable	support

## Rear USB Connector

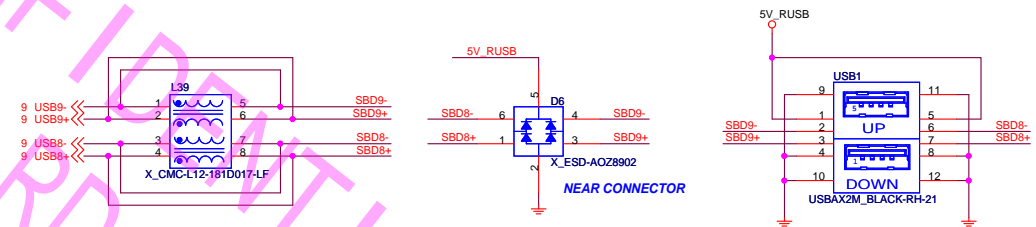
NEAR USB REAR CONNECTOR



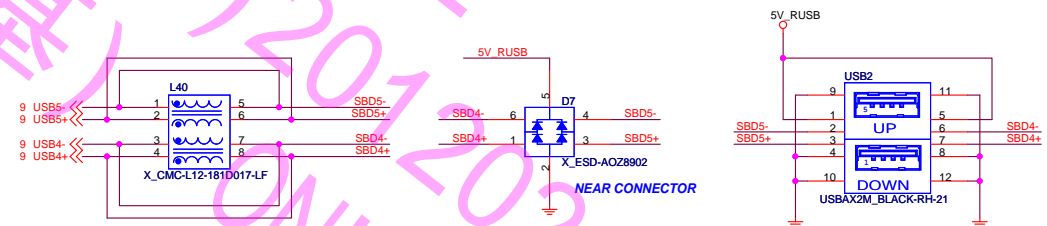
### REAR USB PORT 10,11 (With LAN)



### REAR USB PORT 8,9



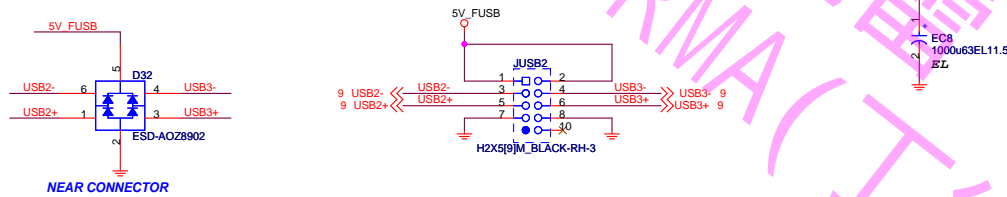
### REAL USB PORT 4,5



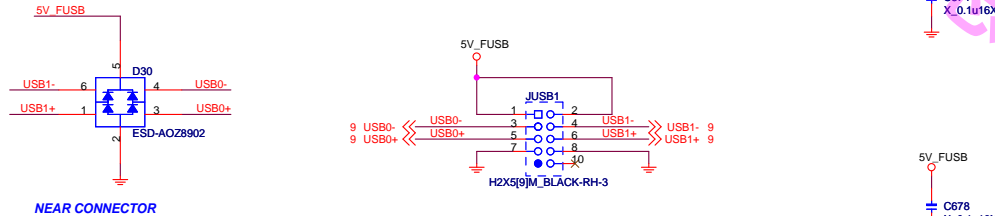
## Front USB Connector

For H61 6,7,12,13 Port should be remove

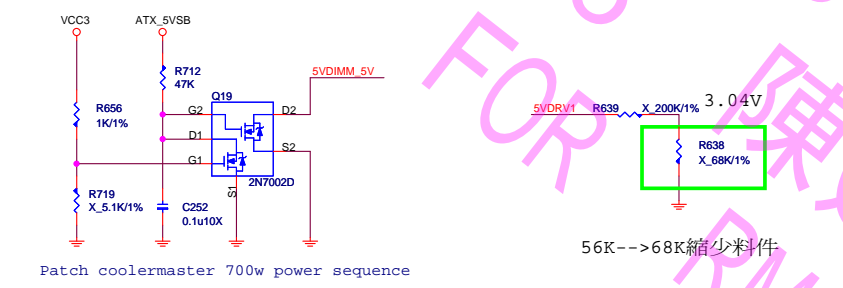
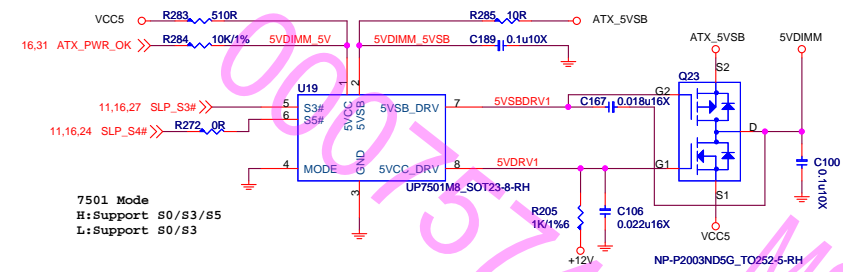
### FRONT USB PORT 2,3



### FRONT USB PORT 0,1

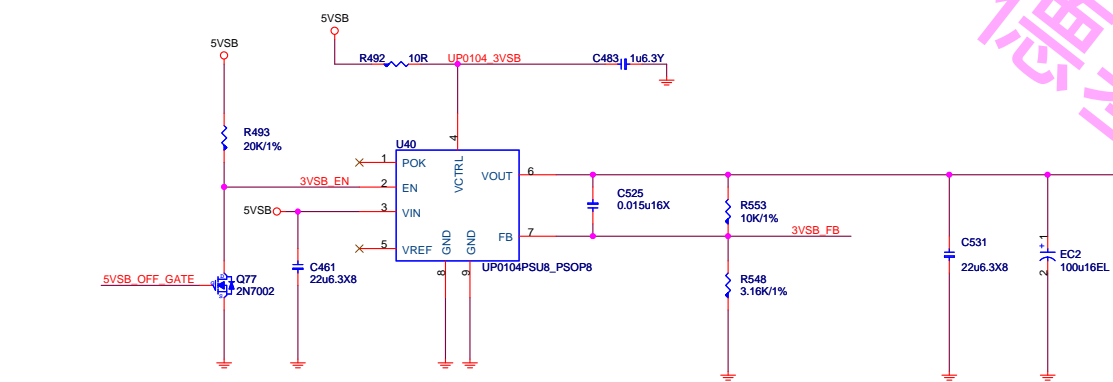


5VDIMM FOR DDR

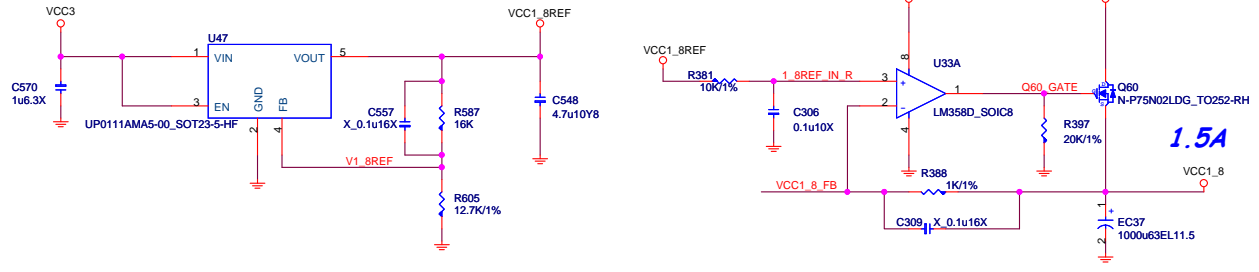


3VSB

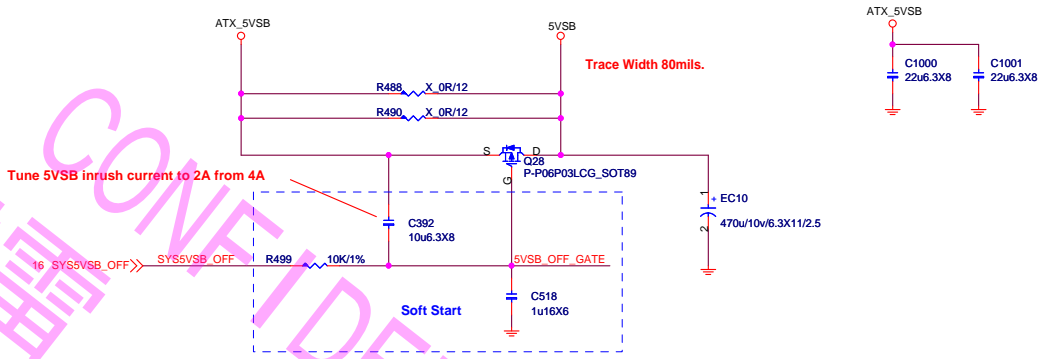
3VSB supply to PCH and other device.  
Turn off when Deep S3/S5 by 5VSB off.



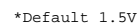
VCC1\_8REF



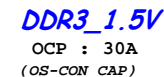
5VSB Power Switch



4.5A FOR CPU  
6A FOR 2DIMM  
1A FOR DDR VTT  
8A FOR PCH

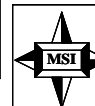
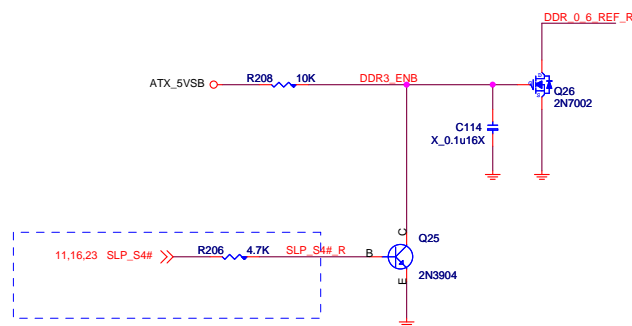
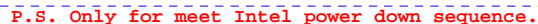


```
DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)
```



### DDR VTT Power

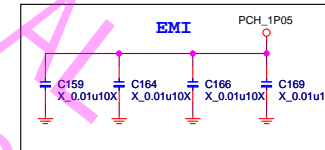
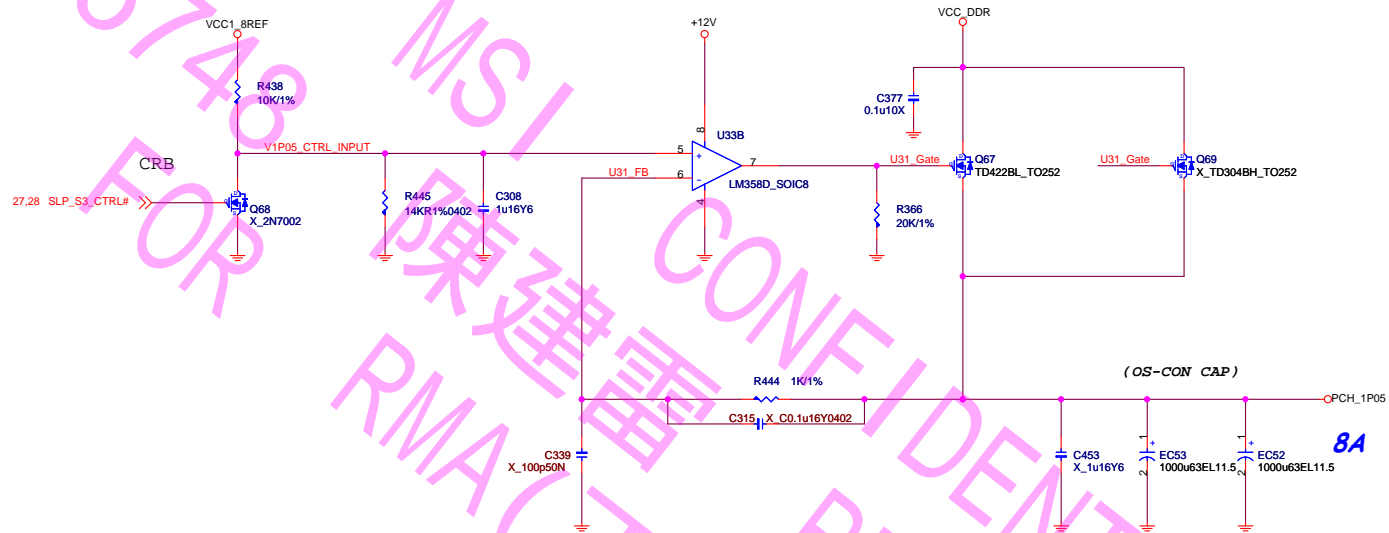
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$0.2075A \times 4 = 0.415A$$


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PCH Power:1.05V



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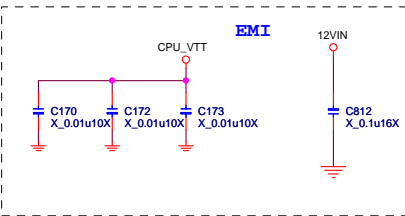
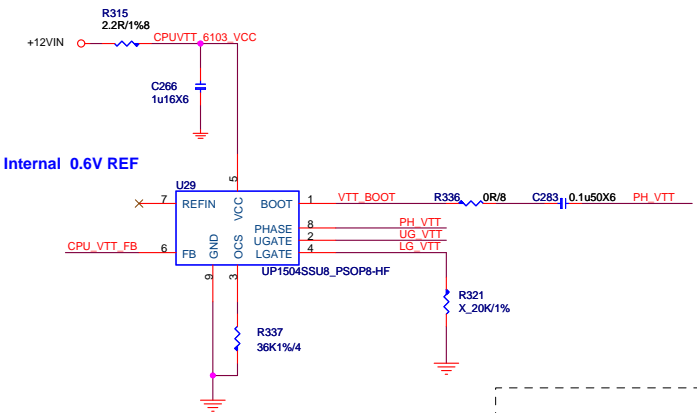
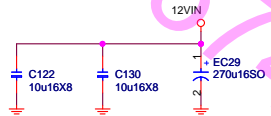
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Custom	PCH Power - OP+MOS	10
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CPU\_VTT:1.05/1.00

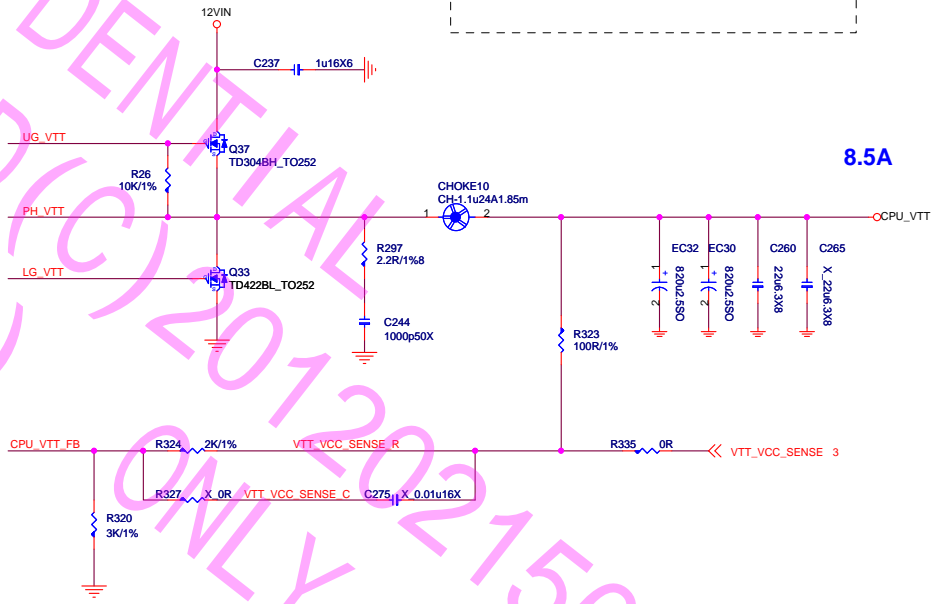
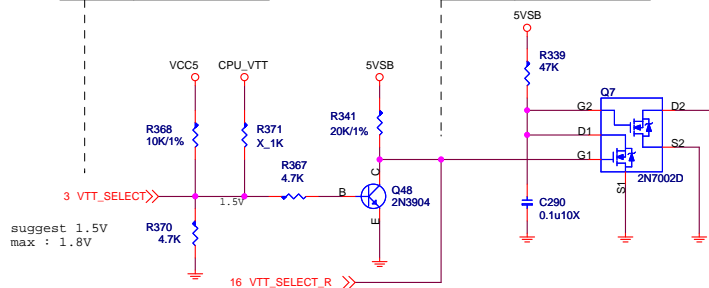
$CPU\ VTT\ 8.5A + SA\ Core = 8.8A = 17.3A$

$I_{ripple} = 1.92(vtt) + 1.88(sa)$   
 $5 \times 1 = 5A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

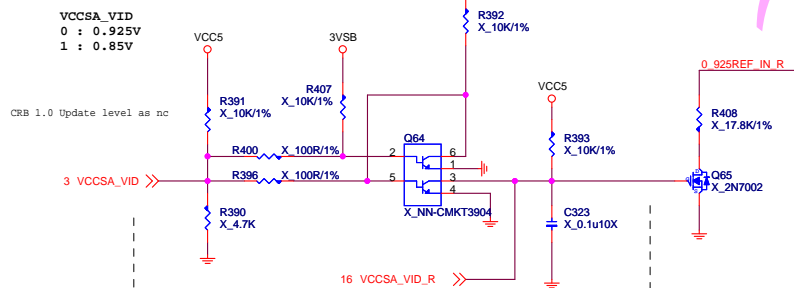
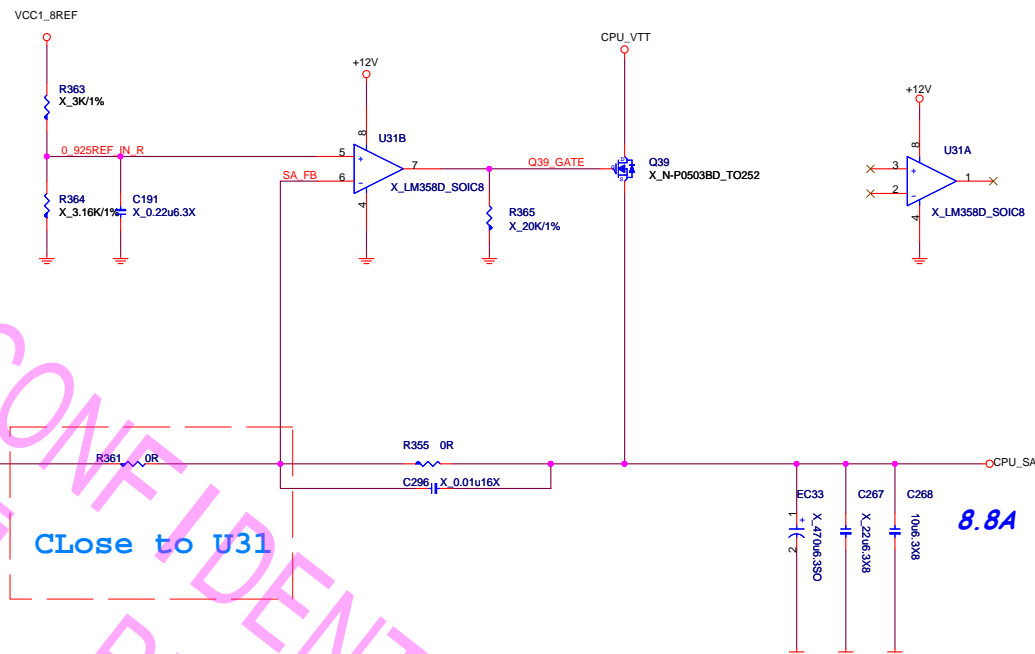
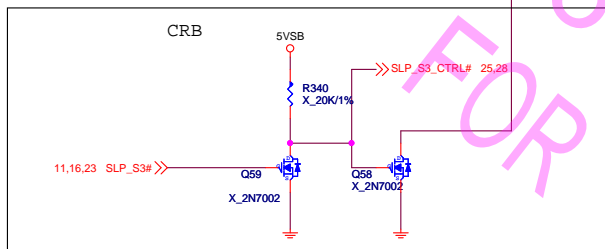
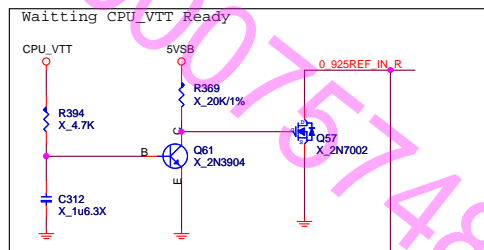
VTT_SELECT Table	
Low	1.05V
High	1.0V





CPU\_SA:0.925/0.85

SA Core = 8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

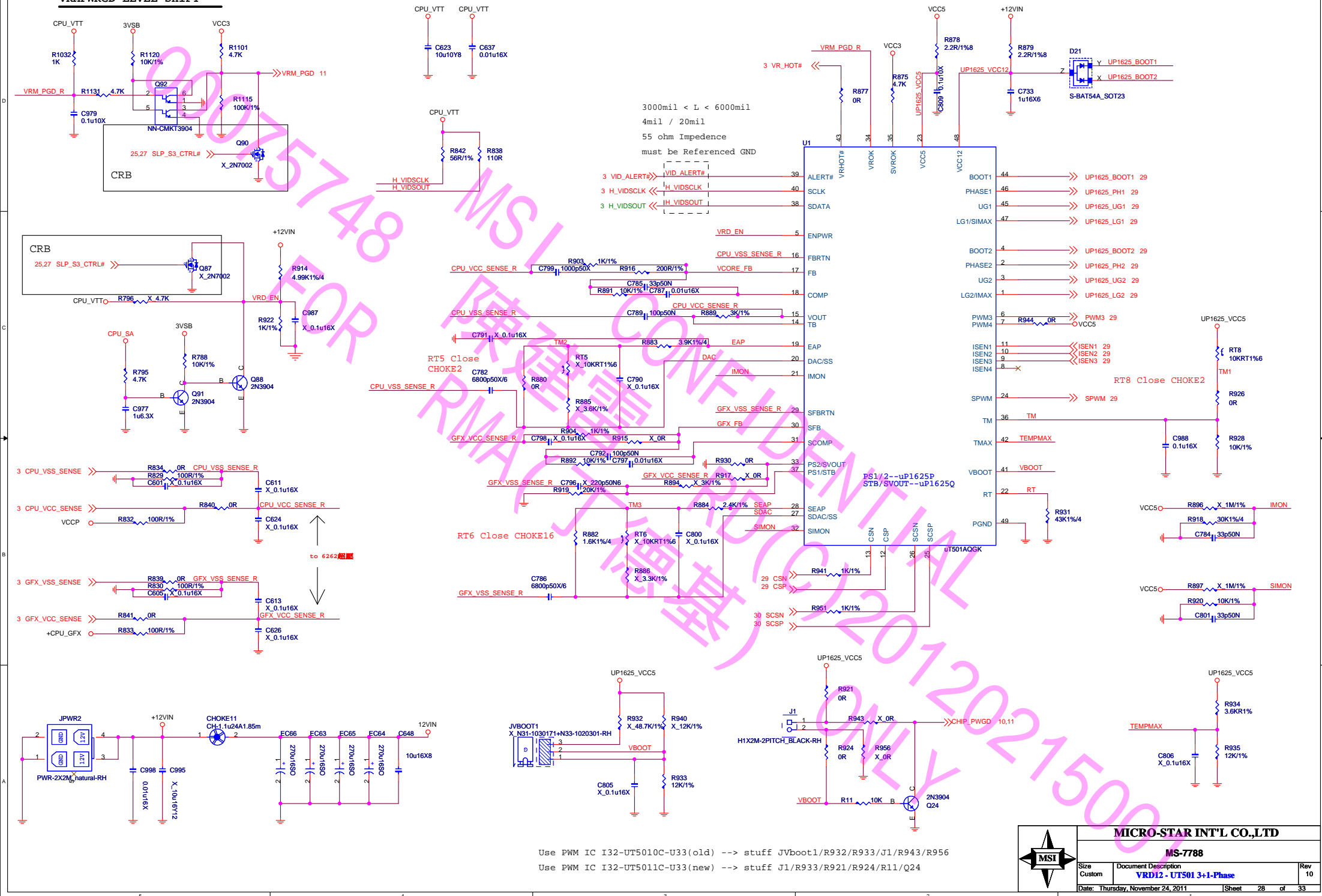


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## VRMPWRGD LEVEL SHIFT



Use PWM IC I32-UT5010C-U33(old) --> stuff JVboot1/R932/R933/J1/R943/R956

Use PWM IC I32-UT5011C-U33(new) --> stuff J1/R933/R921/R924/R11/Q24

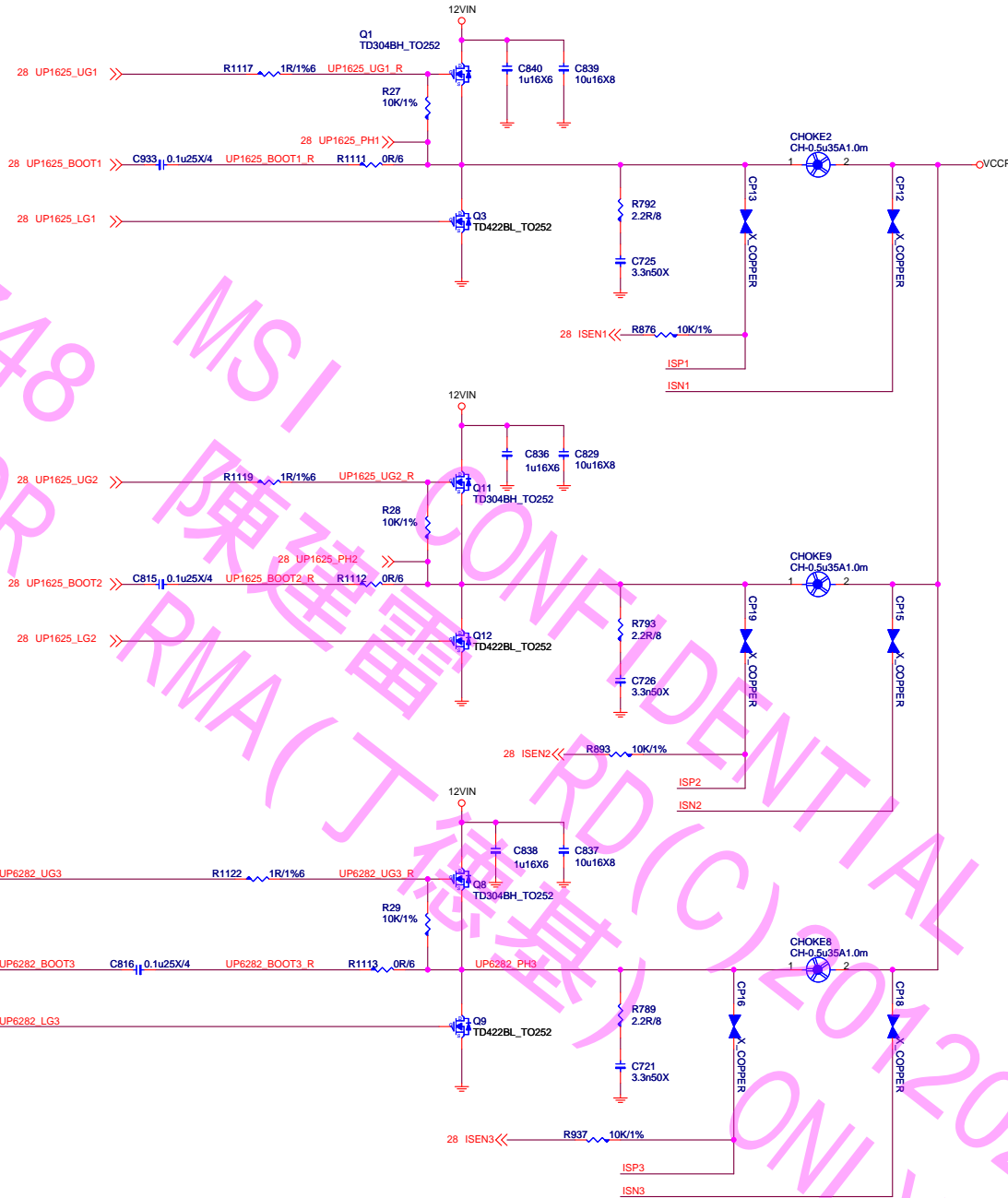
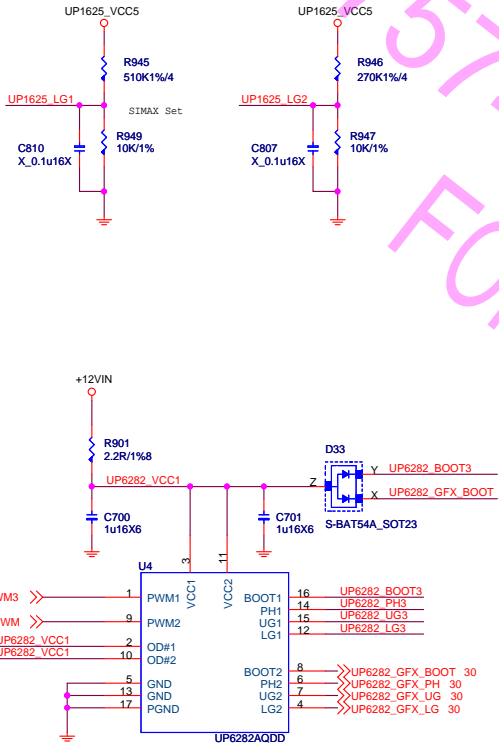


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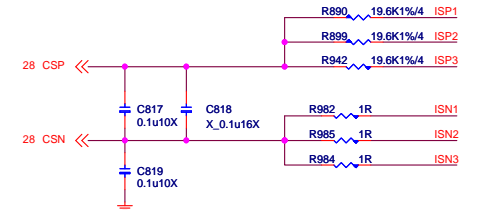
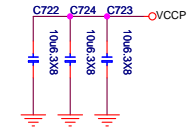
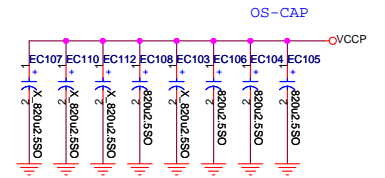
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Size Custom	Document Description <b>VRD12 - UT501 3+1-Phase</b>	Rev 10
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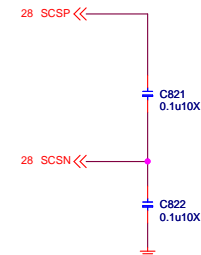
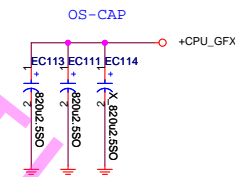
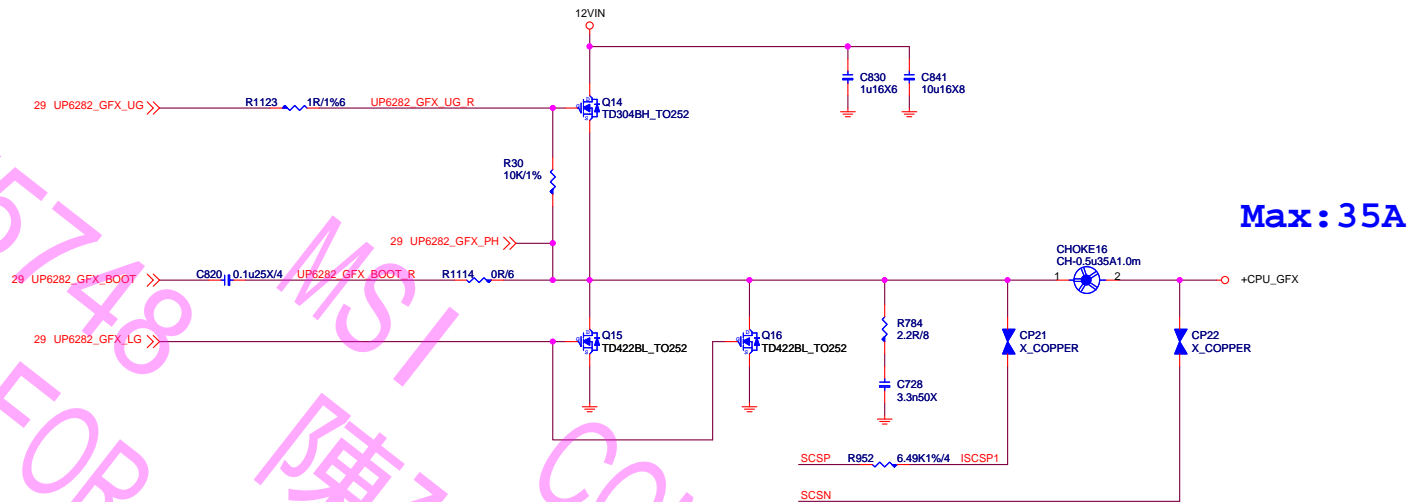
00075748 FOR RMA (丁德基) ONLY 2021500



0.5V~1.6V/110A  
VCORE 75A TDC:55A  
LL:1.7m ohm



00075748 FOR RMA(陳建雷 RD(C)2012021500) ONLY

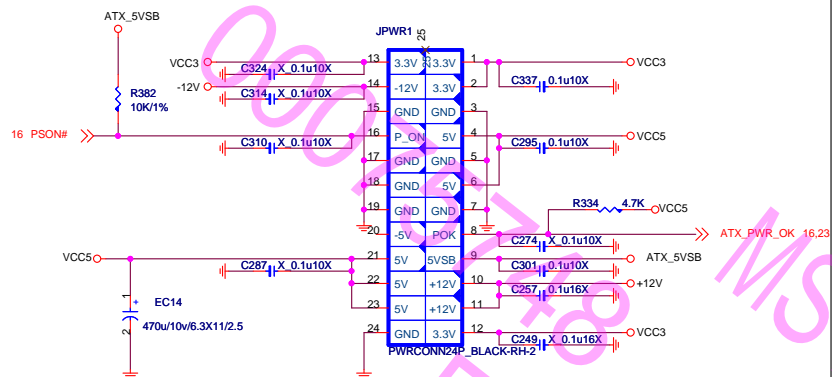


MICRO-STAR INT'L CO.,LTD

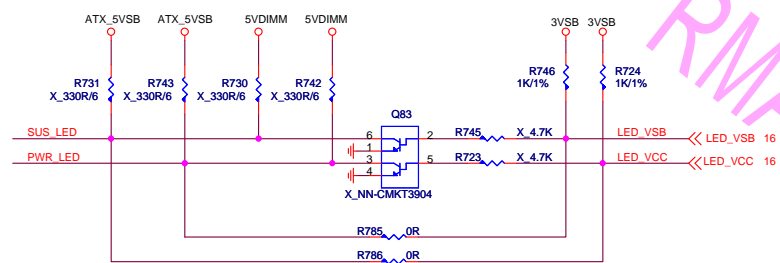
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Custom	UP6234 1-Phase GPU	10
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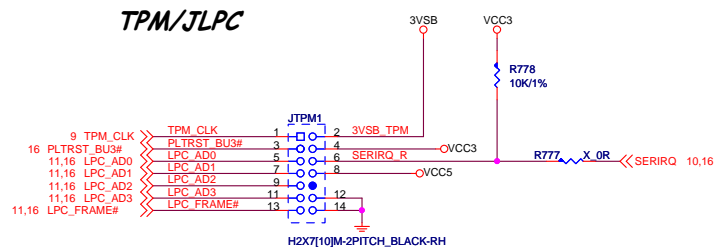
## ATX POWER CONNECTOR



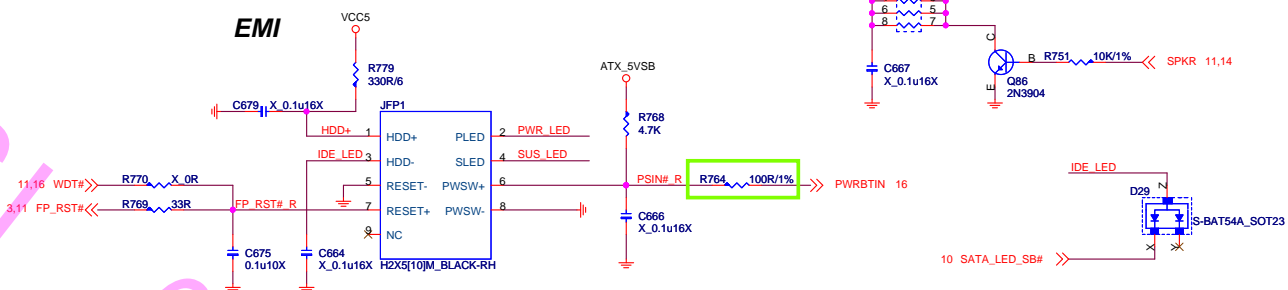
**LED ( for Fintek 71868)**



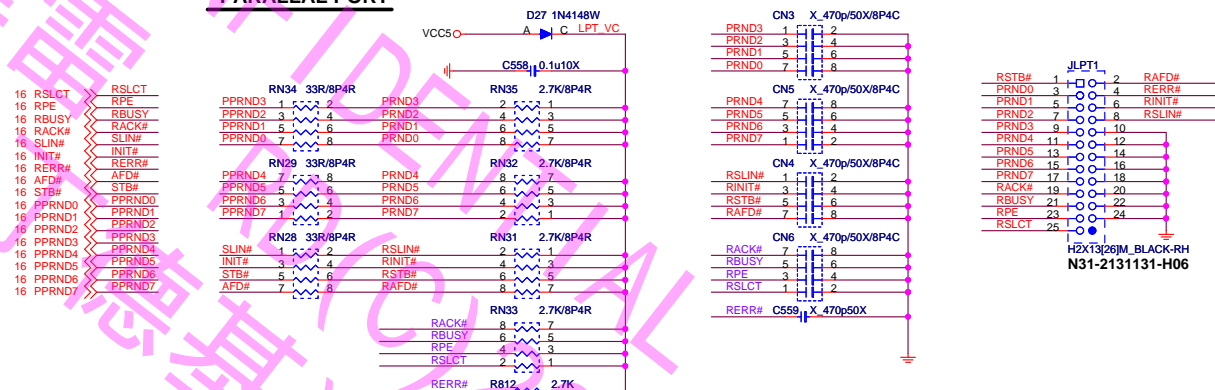
## TPM/JLPC



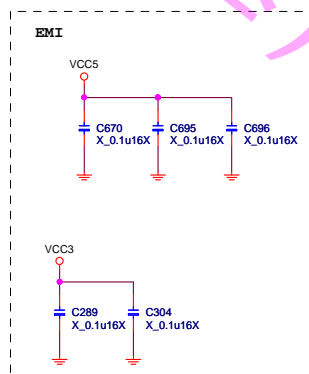
FRONT PANNEL



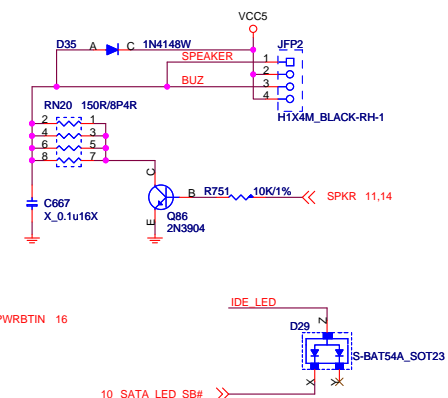
## PARALLAL PORT



## EMI



### Speaker Pin Header



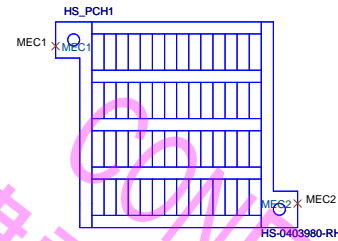
**MICRO-STAR INT'L CO.,LTD**

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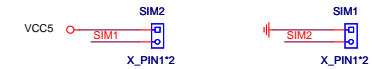
Size Custom	Document Description <b>ATX PWR-Connector &amp; Front Panel &amp; EMI</b>	Rev 10
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## MS-7680-5.1

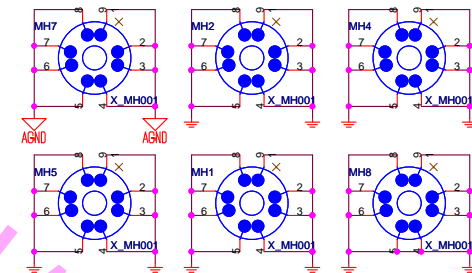
OPT	Configure	BOM	Function
A	H61M-P30 (B3)	601-7680-300	H61M-P30 (B3),H61 B3,2*DDRIII,1*PCI-Ex16,2*PCI-Ex1,Gb Lan,4*SATAII,10*USB2.0,HD 8Ch Audio,DVI/D-sub,All Solid Cap,EuP,RoHS
B	H61M-P20 (B3)	601-7680-20S	H61M-P22 (B3),H61 B3,2*DDRIII,1*PCI-Ex16,2*PCI-Ex1,10/100 Lan,4*SATAII,10*USB2.0,HD 8Ch Audio(3 hole),DVI/D-sub,Half Solid Cap,EuP,RoHS
C	H61M-P25 (B3)	601-7680-310	H61M-P25 (B3),H61 B3,2*DDRIII,1*PCI-Ex16,2*PCI-Ex1,Gb Lan,4*SATAII,10*USB2.0,HD 8Ch Audio(3 hole),DVI/D-sub,Half Solid Cap,EuP,RoHS
D	H61M-P22 (B3)	601-7680-320	H61M-P22 (B3),H61 B3,2*DDRIII,1*PCI-Ex16,2*PCI-Ex1,10/100 Lan,4*SATAII,10*USB2.0,HD 8Ch Audio(3 hole),DVI/D-sub,Half Solid Cap,EuP,RoHS

PCH XDP PWRGD/RESET

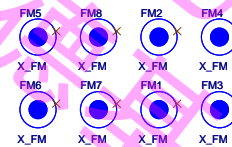
## Simulation



## Mounting Holes



## Optical Fiducial Marks-120



PCB1

7788-10  
PK0-0768051-E36, E&E, 23, 寶安恩斯邁廠 (MSIS), 4, Coffee  
PK0-0768051-E36, E&E, 27, 寶安恩斯邁廠 (MSIS), 4, Coffee  
PK0-0768051-G37, 精成, 23, 寶安恩斯邁廠 (MSIS), 4, Coffee  
PK0-0768051-G37, 精成, 27, 寶安恩斯邁廠 (MSIS), 4, Coffee



BAT1\_X1

BAT-BCR2032P-RH



RUB1

USB




RUB2

USB



CPU\_H1

E21-7557050-L06

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MS-7680 5.1 Change to MS-7778 0A

- 1. 7.1-Channel Audio out change to 5.1-Channel Audio out.
- 2. Remove PCIe X1 slot (PCI\_E3).
- 3. Remove SPIDF out.
- 4. Remove Front USB port\*2 (JUSB3).
- 5. JLPT1 2mm pitch change to 2.54mm pitch.

MS-7788 0A Change to MS-7788 1.0

- 1. modify VT501 COMP & SCOMP not connection to GND.
- 2. Vcore : E110、EC112、EC103、EC107 >> N.C  
C196、C198、C209、C210、C211 >> N.C  
Vtt : C213、C214、C227、C228、C265 >> N.C  
Vgfx : C109、C203、EC114 >> N.C  
PWM : C782、C786 Chang to 6.8nF ; R928 Change to 10K1%  
By Power Solution.
- 3. Add C634、C642、C794、C795、C802 Empty By Audio codec ALC887 co-lay VT1708S CE.
- 4. Add C25 Empty By EMI Solution.
- 5. EC55 & EC56 DIP Footprint Change to SMD DIP Footprint (MSI P/N:C96-1001630-N07) By PM Request.